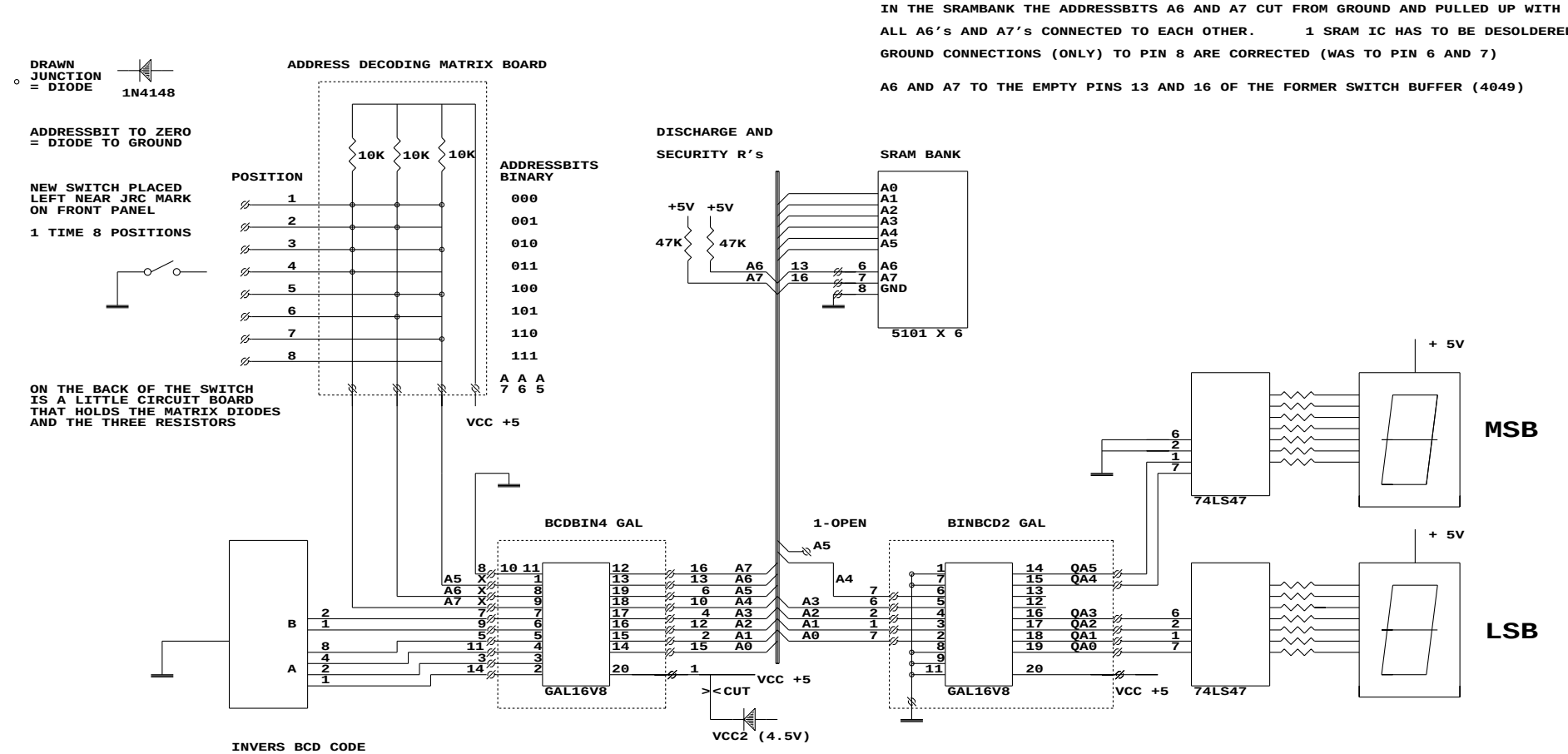

THE TWO DECODING GALS ARE EACH PLACED IN A SOCKET ON A PIECE OF CIRCUIT BOARD
THE BINBCD GAL IS PLACED BETWEEN THE 2 74LS47 IC'S, AND IS CONNECTED IN THE CUT INPUT SIGNALS
THE CHANNELSWITCH BUFFER (4049) IS REMOVED, A SOCKET IS PLACED THERE AND
A PIECE OF FLATCABLE WITH DIL PLUG CONNECTS BETWEEN SOCKET AND GAL BOARD
A6 AND A7 ARE CONNECTED WITH WIREWRAP FROM THE RAMS TO 2 UNUSED FORMER 4049 PINS

W.A.J. GEERAERT PE1ABR

Title: MEMORY CONTROL UPGRADE FOR THE NDH - 515		
Size: B	Document Number: FROM 1 X 24 TO 8 X 24 CHANNELS	REV
Date: December 31, 1999	Sheet of	