Low power dual operational amplifier

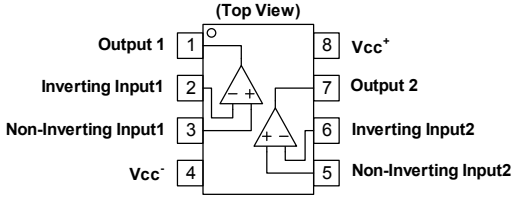
Features

- Internally frequency-compensated
- Large DC voltage gain : 100dB typ.
- Wide bandwidth (unity gain) : 1.1MHz typ.
- Low Operating Current : 350 uA/ch typ.
- Low input bias current: : 20nA typ.
- Low input offset voltage : 0.5mV typ.
- Input common-mode voltage range includes negative rails
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing : 0V to (V_{CC}^+ - 1.5V)
- Internal ESD protection
  Human body model (HBM) ±2000V typ.
- Wide power supply range:
  - Single supply: +3V to +30V
  - Dual supplies: ±1.5V to ±15V

NJM358CG
(SOP8)

NJM358CV
(SSOP8)

Pin connections



Description

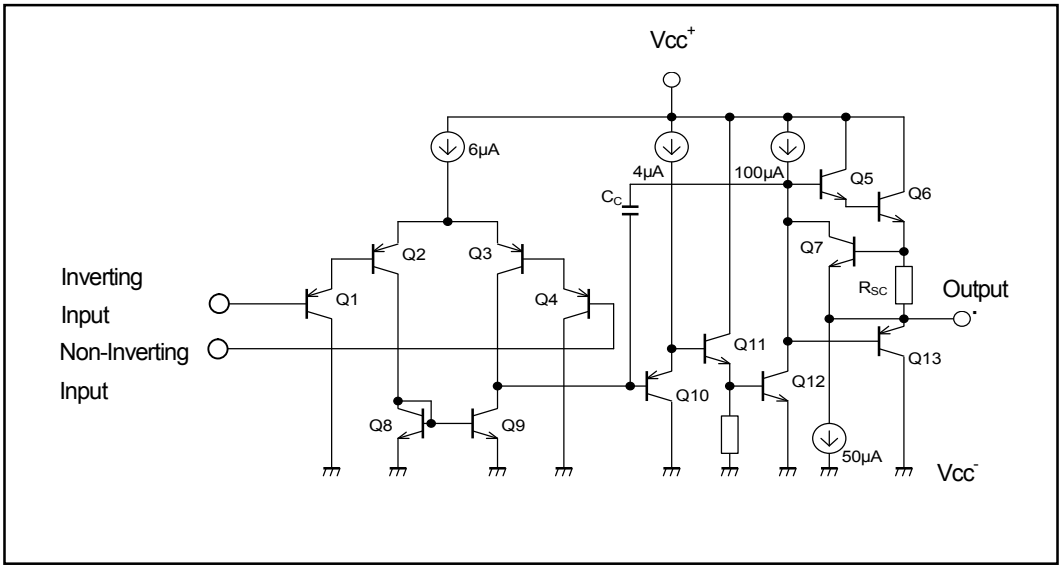
The NJM358C consist of two independent, high-gain, internally frequency-compensated op-amps, specifically designed to operate from a single power supply over a wide range of voltages. The low-power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits, which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard +5V, which is used in logic systems and will easily provide the required interface electronics with no additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

1. Schematic diagram

Figure 1. Schematic diagram (1/2 NJM358C)



2. Absolute maximum ratings and operating conditions

Table1. Absolute maximum ratings

(Tamb=25ºC)

Symbol	Parameter	RATINGS	Unit
V_{CC}	Supply voltage (V_{CC}^+ - V_{CC}^-)	32	V
V_{IN}	Input voltage (1)	Vcc^- -0.3 to Vcc^- +32	V
V_o	Output Terminal Input Voltage	Vcc^- -0.3 to Vcc^+ +0.3	V
V_{ID}	Differential input voltage	±32	V
I_{IN}	Input current (2)	5mA in DC or 50mA in AC (duty cycle = 10%, T=1s)	mA
T_{stg}	Storage temperature range	-65 to +150	ºC
T_j	Maximum junction temperature	150	ºC
P_D	Power Dissipation	SOP8 : 690(4) 1000(5) SSOP8 : 430(4) 540(5)	mW
θja	Thermal resistance junction to ambient(3)	SOP8 : 180(4) 122(5) SSOP8 : 290(4) 230(5)	ºC /W
ψjt	Thermal resistance junction to top surface of IC package(3)	SOP8 : 49(4) 43(5) SSOP8 : 46(4) 45(5)	ºC /W

1. Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of V_{CC}^+
   The normal amplifier operation input voltage is within "Common Mode Input Voltage Range" specified in the Electrical characteristics.
2. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-vase junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.
3. Short-circuit can cause excessive heating and destructive dissipation. Values are typical.
4. EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 2layers, FR-4) mounting
5. EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 4layers, FR-4) mounting

3. Operating conditions

Table2. Operating conditions

(Tamb=25°C)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{CC}^+ - V_{CC}^-)	3 to 30	V
T_{oper}	Operating free-air temperature range	-40 to +85	ºC

4. Electrical characteristics

Table3. V_{CC}^+ = +5V, V_{CC}^- = 0V, T_{amb} = +25˚C , (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1) T_{amb} = 25˚C 0 ºC ≤ T_{amb} ≤ 70 ºC (5)	 - -	 0.5 -	 7 9	mV
DV_{io}	Input offset voltage drift 0 ºC ≤ T_{amb} ≤ 70 ºC (5)	-	7	30	µV/ºC
I_{io}	Input offset current T_{amb} = 25˚C 0 ºC ≤ T_{amb} ≤ 70 ºC (5)	 - -	 2 -	 30 40	nA
DI_{io}	Input offset current drift 0 ºC ≤ T_{amb} ≤ 70 ºC (5)	-	-	300	pA/ºC
I_{ib}	Input bias current (2) T_{amb} = 25˚C 0 ºC ≤ T_{amb} ≤ 70 ºC (5)	 - -	 20 -	 150 200	nA
A_{vd}	Large signal voltage gain (V_{CC}^+ = +15V, RL=2kΩ, Vo=1.4V to 11.4V) T_{amb} = 25˚C 0 ºC ≤ T_{amb} ≤ 70 ºC (5)	 50 25	 100 -	 - -	V/mV
SVR	Supply voltage rejection ratio(V_{CC}^+ = 5V to 30V, Rs<10kΩ) T_{amb} = 25˚C 0 ºC ≤ T_{amb} ≤ 70 ºC (5)	 65 65	 100 -	 - -	dB
I_{CC}	Supply current, all amp, no load 0 ºC ≤ T_{amb} ≤ 70 ºC (5) , V_{CC}^+ = 5V 0 ºC ≤ T_{amb} ≤ 70 ºC (5), V_{CC}^+ = 30V	 - -	 0.7 -	 1.2 2	mA
V_{icm}	Input common mode voltage range(V_{CC}^+ = +30V (3)) T_{amb} = 25 ºC 0 ºC ≤ T_{amb} ≤ 70 ºC (5)	 0 0	 - -	 V_{CC}^+ - 1.5 V_{CC}^+ - 2	V

Table3. V_{CC}^+ = +5V, V_{CC}^- = 0V, T_{amb} = +25˚C , (unless otherwise specified)

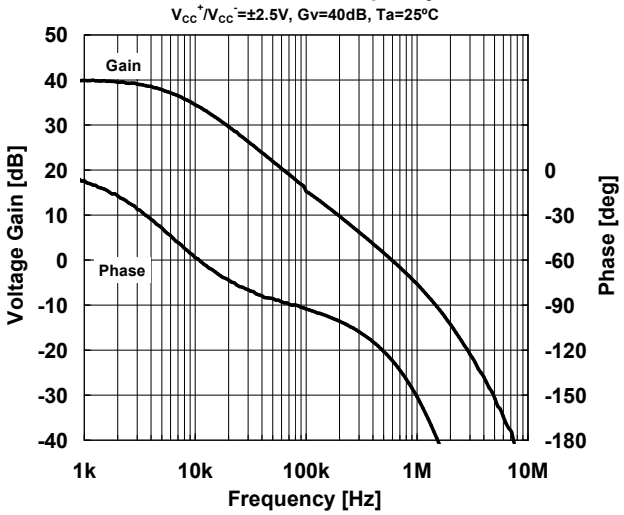
Symbol	Parameter	Min.	Typ.	Max.	Unit
CMR	Common mode rejection ratio(R_S < 10kΩ)				
	T_{amb} = 25°C	70	100	-	dB
	0 ºC ≤ T_{amb} ≤ 70 ºC (5)	60	-	-	
I_{source}	Output current source	20	40	-	mA
	V_{CC}^+ = 15V, V_O = +2V, V_{id} = +1V				
I_{sink}	Output sink current				
	V_{CC}^+ = 15V, V_o = +2V, V_{id} = -1V	10	20	-	mA
	V_{CC}^+ = 15V, V_o = +0.2V, V_{id} = -1V	12	50	-	µA
V_{OH}	High level output voltage(V_{CC}^+ = 30V)				
	T_{amb} = 25°C,R_L = 2kΩ	26	27	-	
	0 ºC ≤ T_{amb} ≤ 70 ºC (5) ,R_L = 2kΩ	26	-	-	V
	T_{amb} = 25°C,R_L = 10kΩ	27	28	-	
	0 ºC ≤ T_{amb} ≤ 70 ºC (5) ,R_L = 10kΩ	27	-	-	
V_{OL}	Low level output voltage				
	T_{amb} = 25°C,R_L = 10kΩ	-	5	20	mV
	0 ºC ≤ T_{amb} ≤ 70 ºC (5) ,R_L = 10kΩ	-	-	20	
SR	Slew rate	-	0.6	-	V/µs
	V_{CC}^+ = 15V, V_i=0.5 to 3V, R_L = 2kΩ,				
	C_L = 100pF, unity gain				
GBP	Gain bandwidth product	-	1.1	-	MHz
	V_{CC}^+ = 30V, f = 100kHz, V_{in}=10mV,				
	R_L = 2kΩ, C_L = 100pF				
THD	Total harmonic distortion	-	0.02	-	%
	f = 1kHz, A_V=20dB, R_L = 2kΩ, V_O = $2V_{pp}$,				
	C_L = 100pF				
e_n	Equivalent input noise voltage	-	30	-	nV/√Hz
	f = 1kHz, R_S=100Ω, V_{CC}^+ = 30V				
V_{O1}/V_{O2}	Channel separation (4)	-	120	-	dB
	1kHz < f < 20kHz				

1. V_O = 1.4V, R_S=0Ω, 5V < V_{CC}^+ < 30V, 0 < V_{ic} < V_{CC}^+ - 1.5V.
2. The direction of the input current is out of the IC.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components, ensure that stray capacitance between these external parts dose not cause coupling.
5. This parameter is not 100% test.

■ TYPICAL CHARACTERISTICS

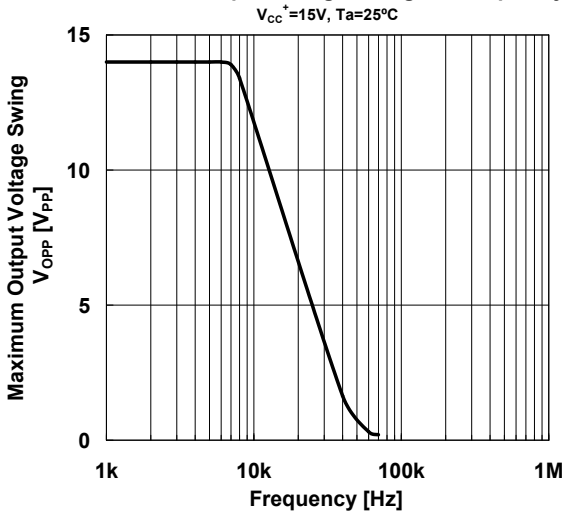
Gain/Phase vs. Frequency

V_{CC}^+/V_{CC}^-=±2.5V, Gv=40dB, Ta=25ºC



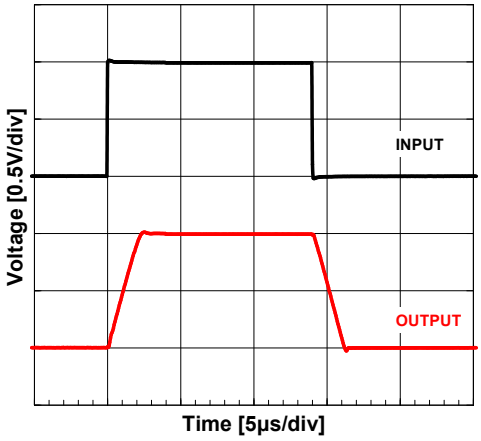
Maximum Output Voltage Swing vs. Frequency

V_{CC}^+=15V, Ta=25ºC



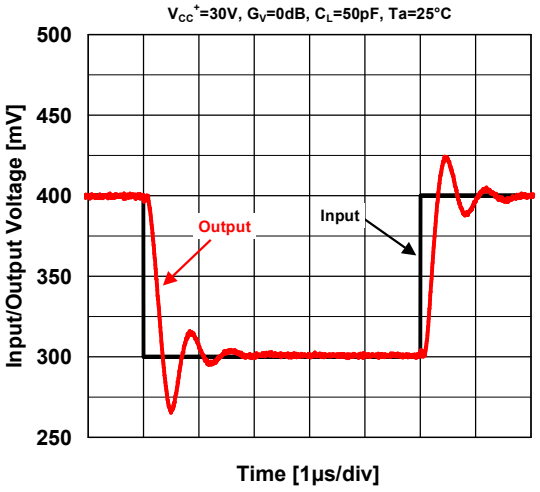
Pulse Response

V_{CC}^+=15V, R_L=2kΩ, C_L=100pF, Ta=25ºC



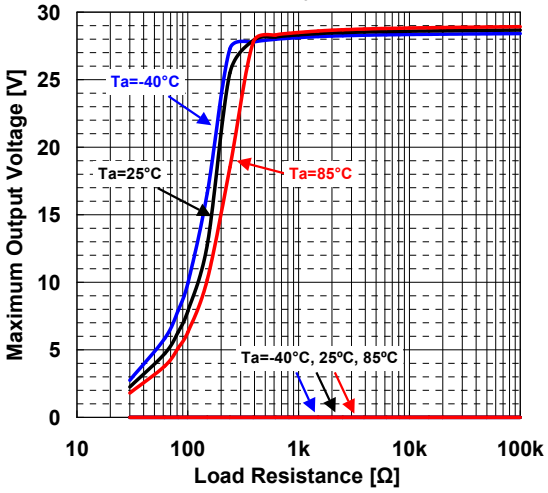
Small signal Pulse Response

V_{CC}^+=30V, G_V=0dB, C_L=50pF, Ta=25°C



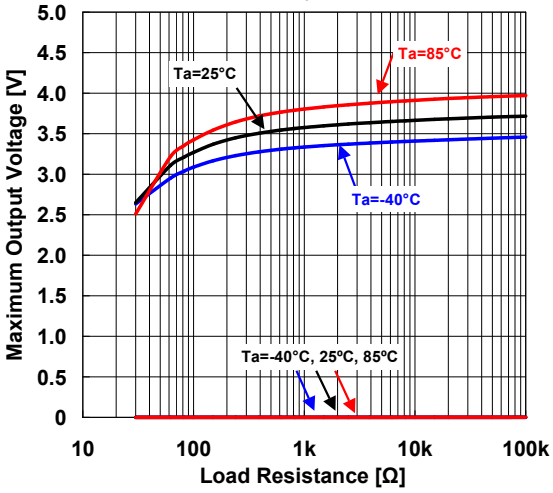
Maximum Output Voltage vs. Load Resistance

V_{CC}^+=30V, Gv=open, R_L to V_{CC}^-



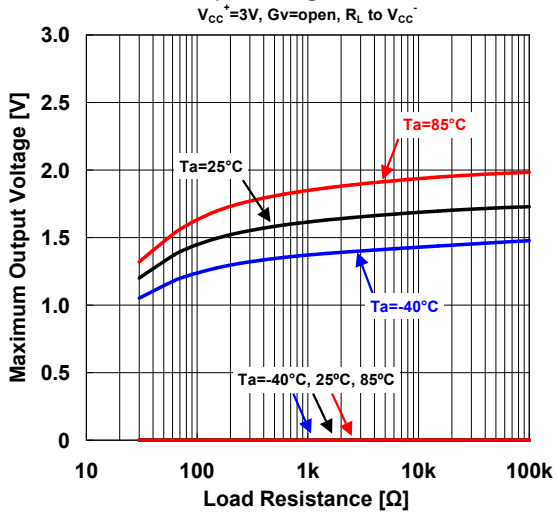
Maximum Output Voltage vs. Load Resistance

V_{CC}^+=5V, Gv=open, R_L to V_{CC}^-

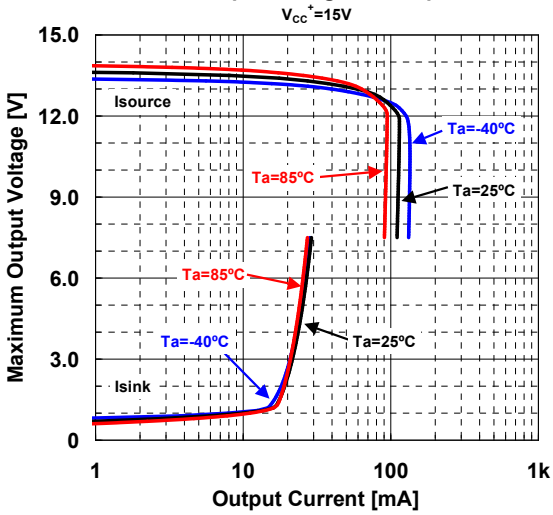


■ TYPICAL CHARACTERISTICS

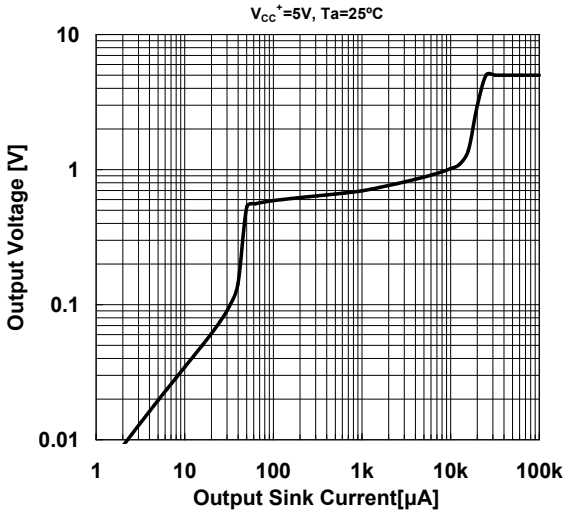
Maximum Output Voltage vs. Load Resistance



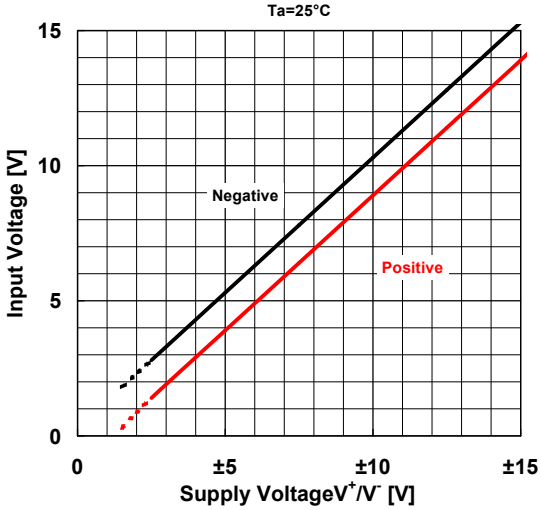
Maximum Output Voltage vs. Output Current



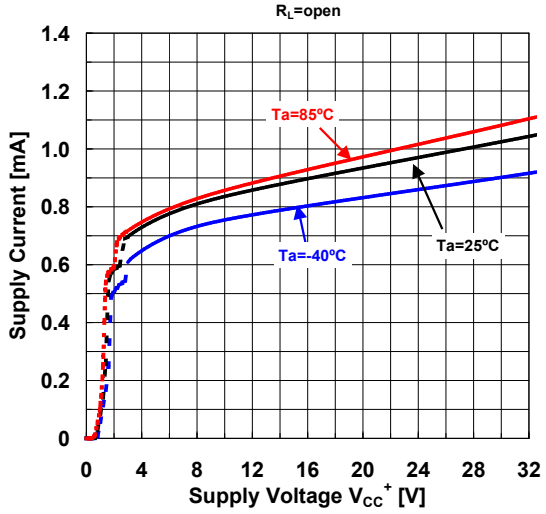
Output Voltage vs. Output Sink Current



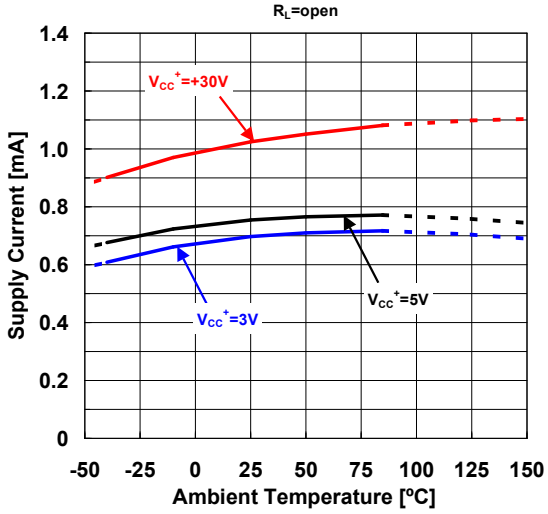
Input Voltage Range vs. Supply Voltage



Supply Current vs. Supply Voltage

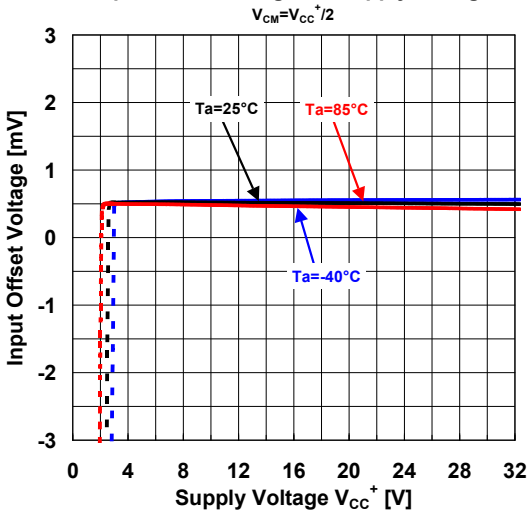


Supply Current vs. Temperature

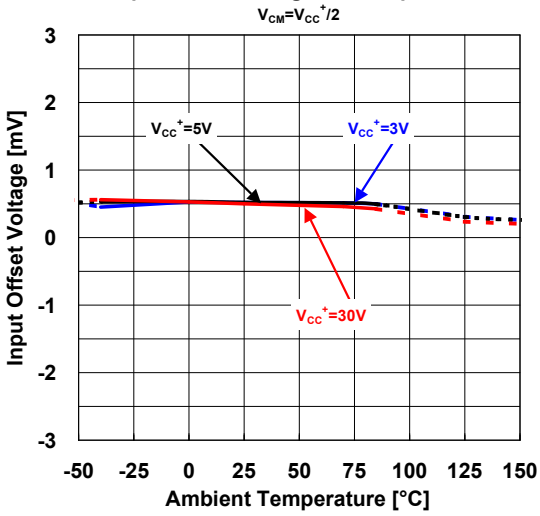


■ TYPICAL CHARACTERISTICS

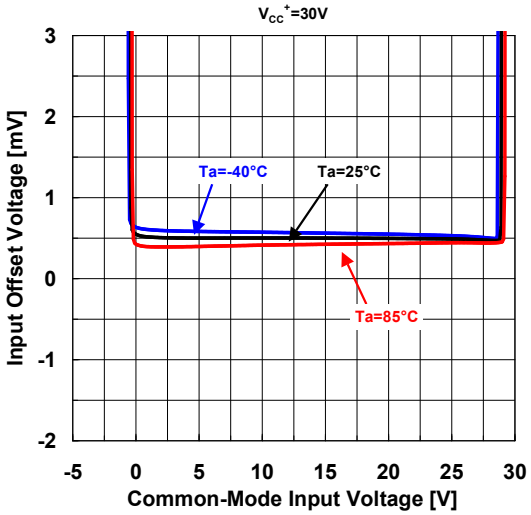
Input Offset Voltage vs. Supply Voltage



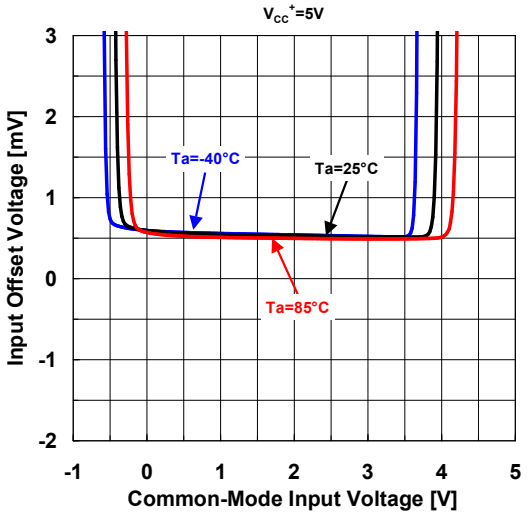
Input Offset Voltage vs. Temperature



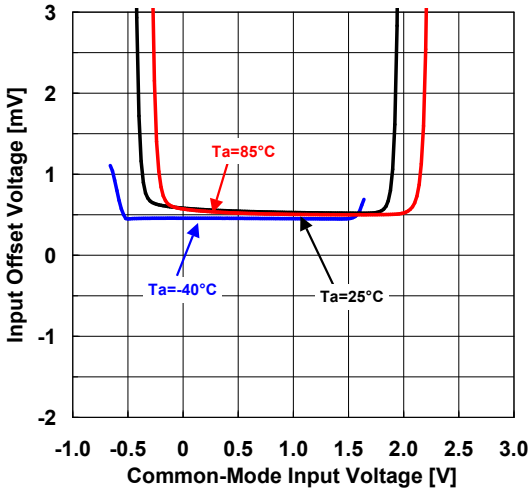
Input Offset Voltage vs. Common-Mode Input Voltage



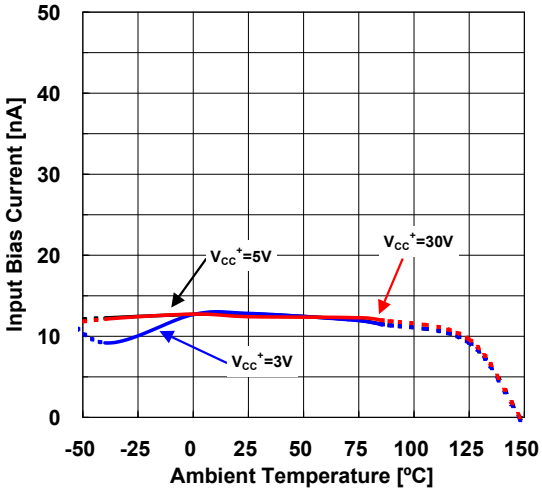
Input Offset Voltage vs. Common-Mode Input Voltage



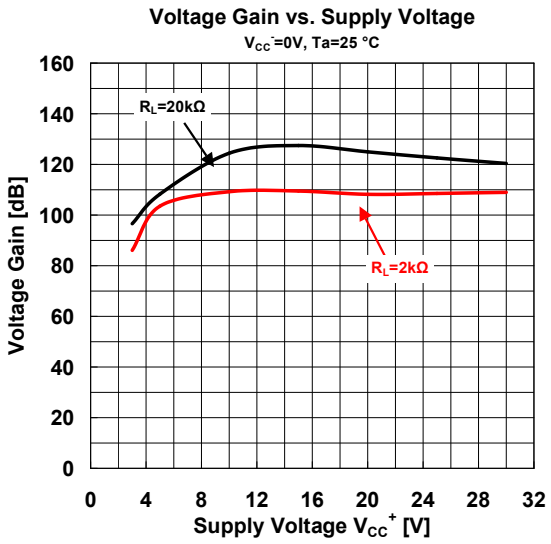
Input Offset Voltage vs. Common-Mode Input Voltage

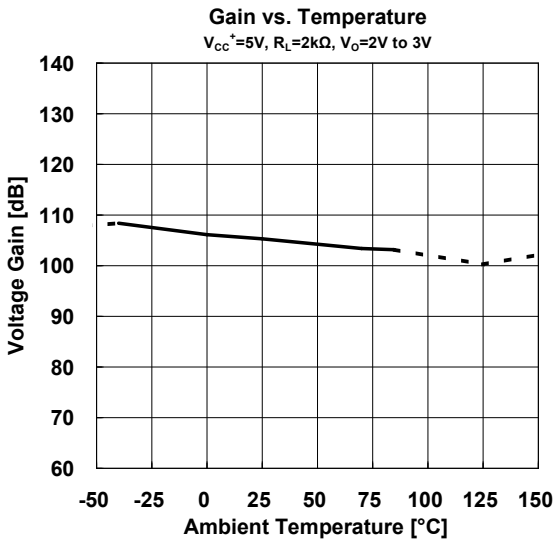


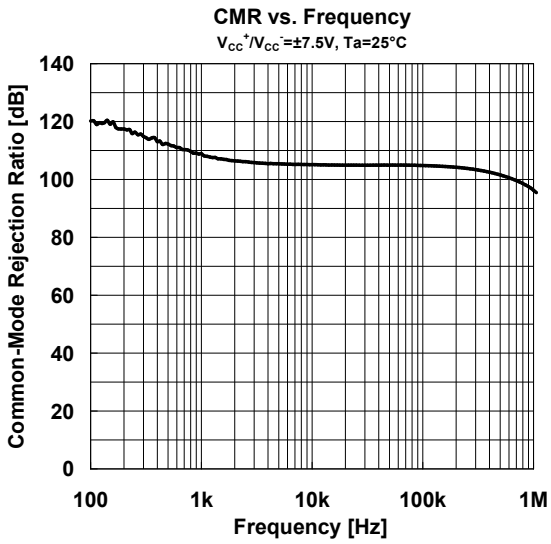
Input Bias Current vs. Temperature

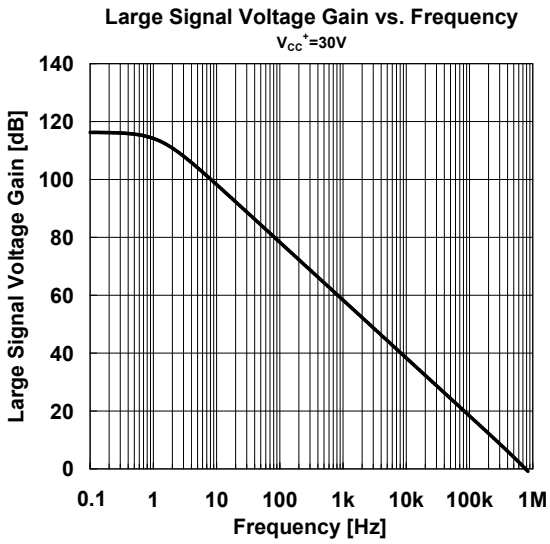


■ TYPICAL CHARACTERISTICS



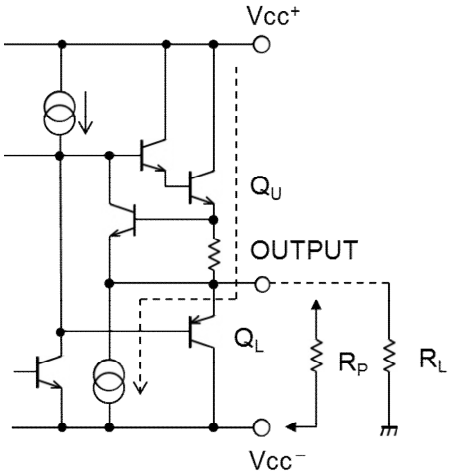






■ APPLICATION

Improvement of Cross-over Distortion
Equivalent circuit at the output stage

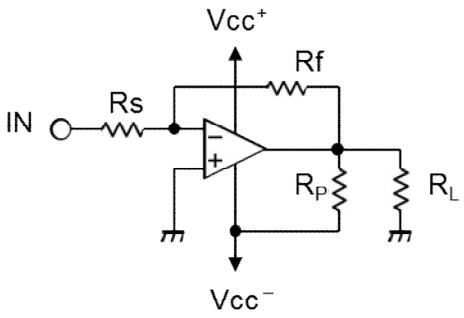


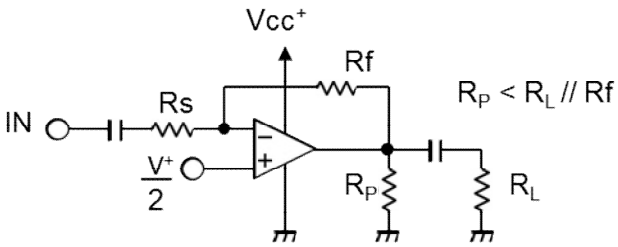
NJM2904C,in its static state (No in and output condition) when design,Q_U being biassed by constant current (break down beam) yet,Q_L stays OFF.

While using with both power source mode,the cross-over distortion might occur instantly when Q_L ON.

There might be cases when application for amplifier of audio signals,not only distortion but also the apparent frequency bandwidth being narrowed remarkably.

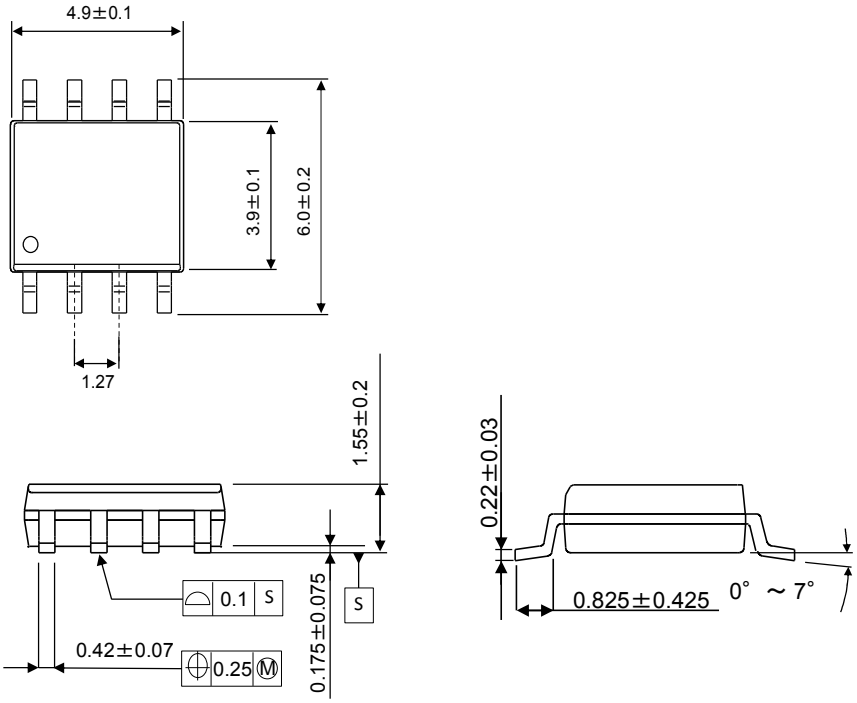
It is adjustable especially when using both power source mode,constantly to use with higher current on Q_U than the load current (including feedback current),and then connect the pull-down resister R_P at the part between output and V⁻ pins.



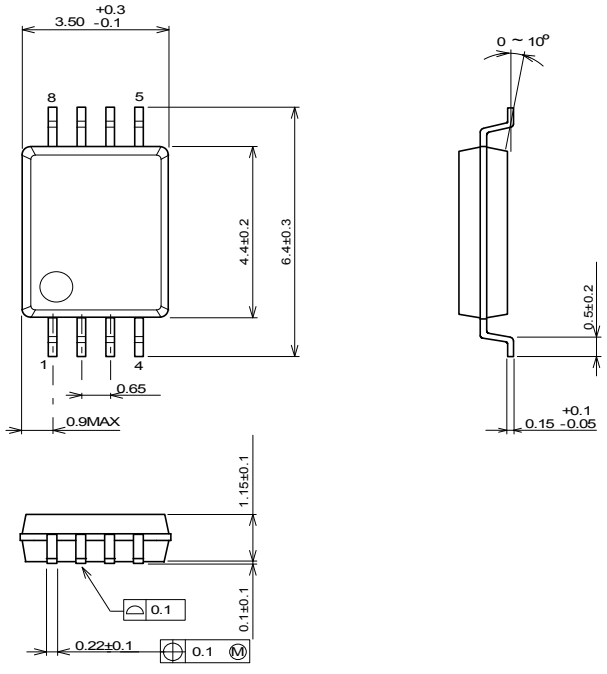


■ PACKAGE DIMENSIONS

SOP8



SSOP8



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