Telecom microcontroller with serial I/O interface

PCD3343A PCD3348A

1 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 3 kbytes ROM, 224 bytes RAM (PCD3343A)
- 8 kbytes ROM, 256 bytes RAM (PCD3348A)
- Serial I/O interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
  - SIO/derivative
- Two test inputs, one of which also serves as the external interrupt input
- Power-on reset
- Stop and Idle modes
- Logic supply voltage: V_{DD} = 1.8 to 6 V
- Low stand-by voltage: V_{DD} = 1 V
- Low stand-by current: I_{DD} = 2 µA typical
- Clock frequency: 1 to 16 MHz
- Oscillator with output drive for peripherals (e.g. PCD3312 DTMF generator)
- Operating temperature: –25 to +70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3343A and PCD3348A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the *"PCD33XXA family data sheet"*, which should be read in conjunction with this publication.

The PCD3343A and PCD3348A are microcontrollers intended for telecom applications. They provide 3 and 8 kbytes of program memory and 224 and 256 bytes of RAM, respectively. In addition to 20 I/O port lines, the microcontrollers provide an on-chip serial I/O interface.

This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I²C-bus devices of the PCF85XX, PCD33XX and 'Clips' peripheral families. These include liquid crystal display drivers, pulse and/or DTMF diallers, ringers, AD/DA converters, clock/calendar circuits, EEPROM and RAM.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3343AP	28	DIP	plastic	SOT117-1
PCD3348AP	28	DIP	plastic	SOT117-1
PCD3343AT	28	SO28L	plastic	SOT136-1
PCD3348AT	28	SO28L	plastic	SOT136-1

4 BLOCK DIAGRAM

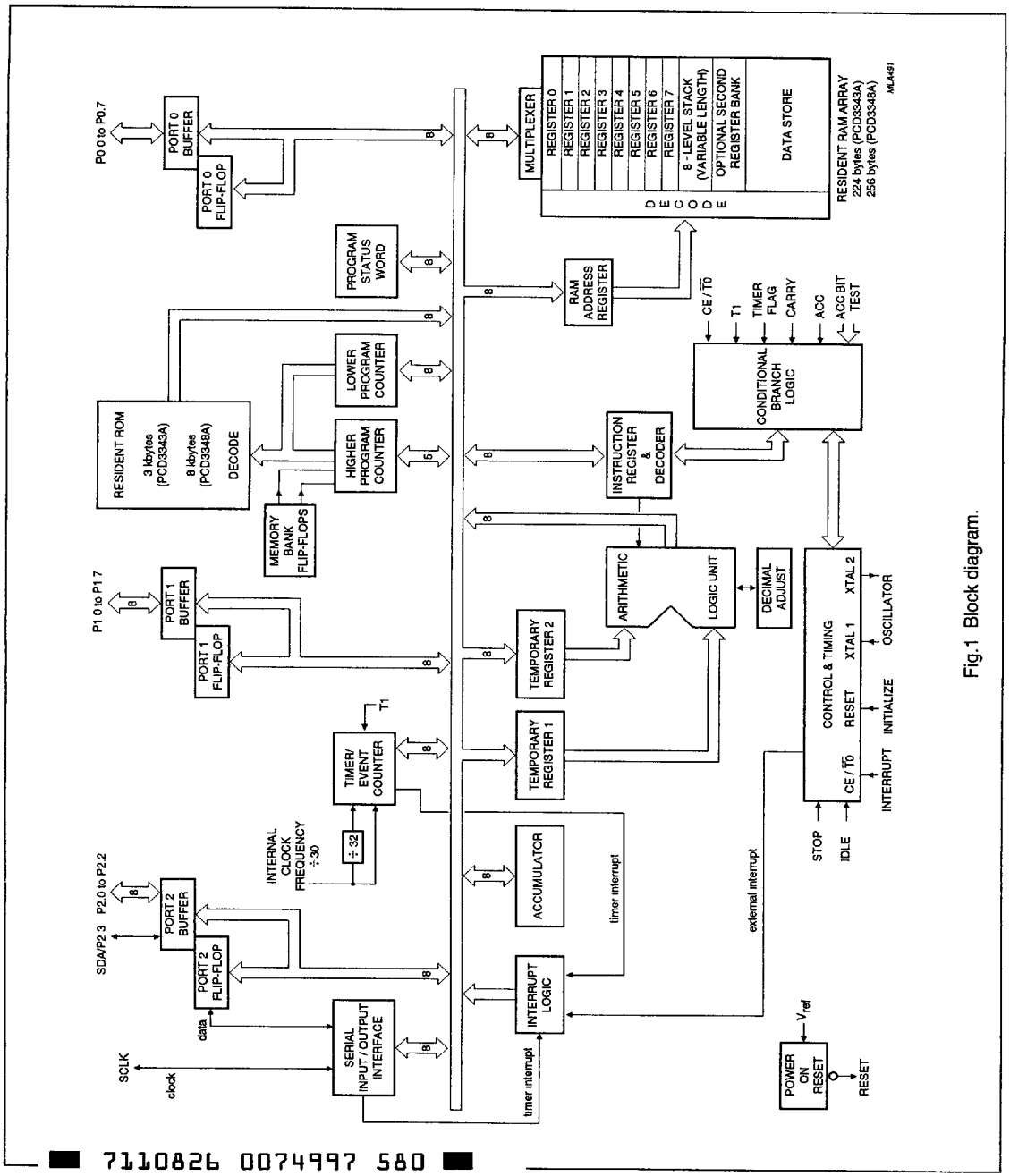


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

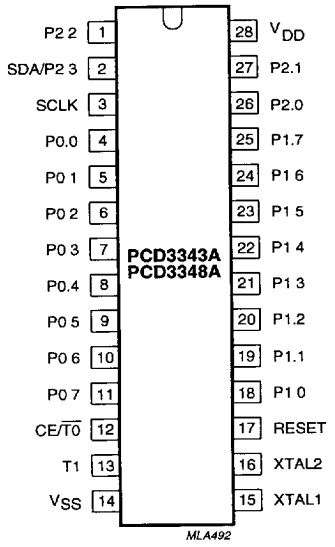


Fig.2 Pin configuration.

5.2 Pin description

Table 1 DIP28 and SO28L packages.

SYMBOL	PIN	TYPE	DESCRIPTION
P2.2	1	I/O	Port 2: quasi-bidirectional I/O line
SDA/P2.3	2	I/O	bidirectional data line of the serial I/O interface/ Port 2: quasi-bidirectional I/O line
SCLK	3	I/O	bidirectional clock line of the serial I/O interface
P0.0 to P0.7	4 to 11	I/O	Port 0: quasi-bidirectional I/O lines
CE/$\overline{T0}$	12	I	Chip Enable/Test 0
T1	13	I	Test 1/count input of 8-bit timer/event counter 1
V_{SS}	14	P	ground
XTAL1	15	I	crystal oscillator/external clock
XTAL2	16	O	crystal oscillator output
RESET	17	I	Reset input
P1.0 to P1.7	18 to 25	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 to P2.1	26 and 27	I/O	Port 2: quasi-bidirectional I/O lines
V_{DD}	28	P	positive supply

6 INSTRUCTION SET

The PCD3343A has ROM space restricted to 3 kbytes. The instructions SEL MB1/2/3 would therefore define non-existing program memory banks and should be avoided. Additionally, RAM space is restricted to 224 bytes for the PCD3343A, so care should be taken to avoid accesses to non-existing RAM locations.

7 SUMMARY OF MASK OPTIONS

Table 2 Port mask options (see *"PCD33XXA family data sheet"*).

PORT	PORT OUTPUT[1]			PORT STATE AFTER RESET	
	OPTION 1	OPTION 2	OPTION 3	SET	RESET
P0.0 to P0.7	X	X	X	X	X
P1.0 to P1.7	X	X	X	X	X
P2.0 to P2.3	X	X	X	X	X
SDA /P2.3	–	X	–	X	–

Note

1. Option 1: normal port
   Option 2: open drain
   Option 3: push-pull.

Table 3 Mask options.

FEATURE	DESCRIPTION
ROM Code: program/data	Any mix of instructions and data up to ROM size of 3 kbytes (PCD3343A) and 8 kbytes (PCD3348A).
Power-on reset voltage level: V_{ref}	1.2 to 3.6 V in increments of 100 mV; OFF
Oscillator transconductance: g_m	LOW transconductance: g_{mL}
	MEDIUM transconductance: g_{mM}
	HIGH transconductance: g_{mH}

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	–	90	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

10 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.579545 MHz (g_{mL}); $R_X \leq 100\ \Omega$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 3 to 8)						
V_{DD}	operating supply voltage	note 1	1.8	–	6	V
V_{DD}	RAM data retention Stop mode		1.0		6	V
I_{DD}	operating supply current	V_{DD} = 3 V; note 1	–	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL}); note 1	–	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM}); note 1	–	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); note 1	–	2.5	6.0	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} = 3 V; note 1	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL}); note 1	–	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM}); note 1	–	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); note 1	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 2	–	1.2	2.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 2	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	+1	µA
Outputs (see Figs 9 to 12)						
I_{OL}	LOW level port sink current except SDA/P2.3 and SCLK	V_{DD} = 3 V; V_O = 0.4 V	0.7	8	–	mA
I_{OL}	LOW level SIO sink current SDA/P2.3 and SCLK	V_{DD} = 3 V; V_O = 0.4 V	1.5	8	–	mA
I_{OH}	HIGH level port pull-up source current	V_O = 2.7 V; V_{DD} = 3 V	−10	−20	–	µA
		V_O = 0 V; V_{DD} = 3 V	–	−100	−300	µA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	−0.7	−4	–	mA
ΔV_{POR}	power-on reset level variation around chosen V_{POR}	note 3	−0.5	0	+0.5	V

Notes

1. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs open. Maximum values: external clock at XTAL1; XTAL2 open. Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; RESET, T1 and CE/$\overline{T0}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; all other outputs open.
3. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.

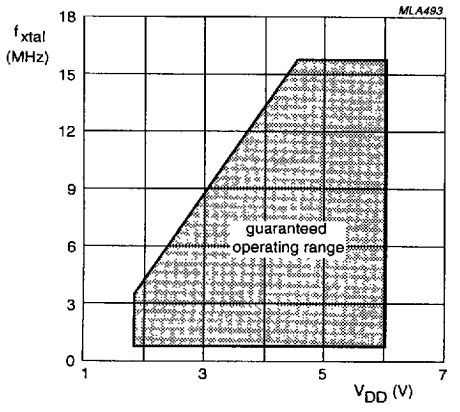


Fig.3 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

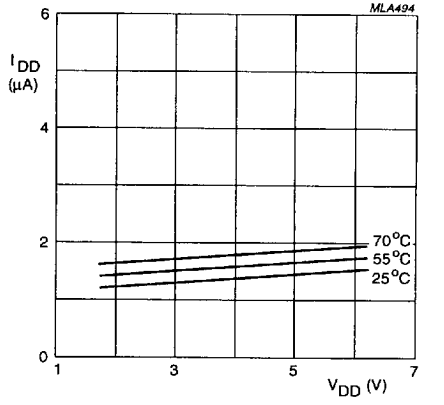


Fig.4 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).

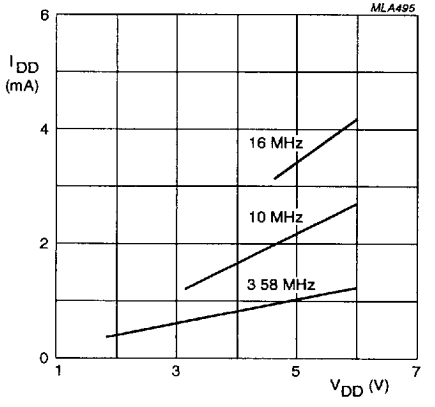


Fig.5 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).

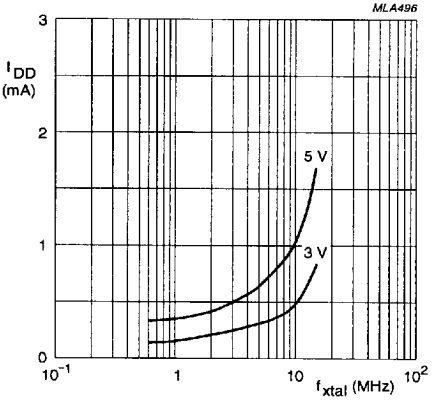


Fig.6 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).

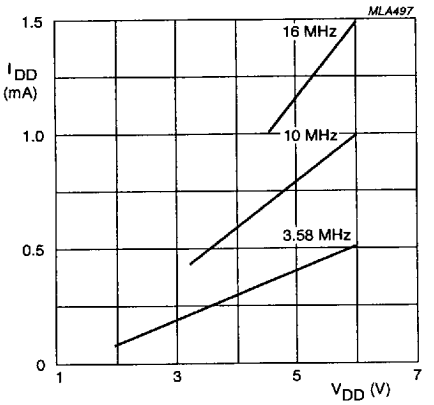


Fig.7 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).

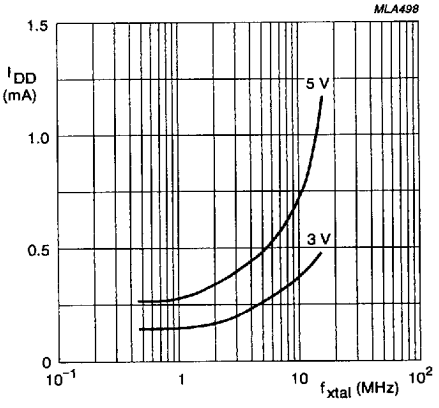
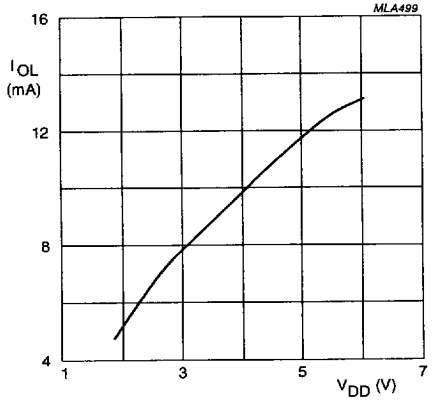
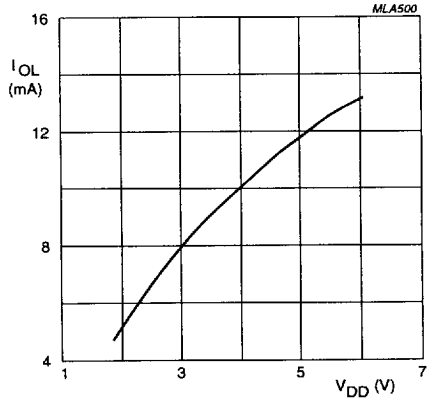


Fig.8 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



V_O = 0.4 V

Fig.9 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.10 Typical SDA/P2.3 or SCLK LOW level output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

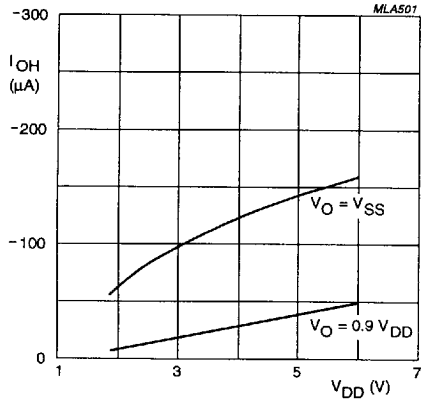
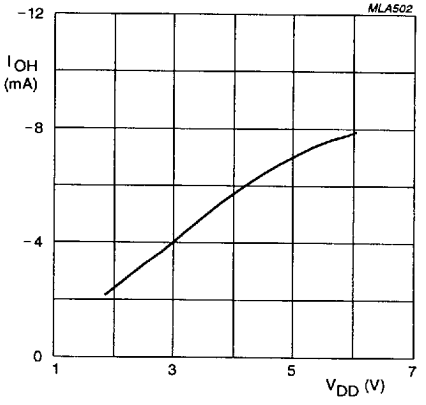


Fig.11 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V

Fig.12 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

11 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified. V_{IL} = V_{SS}; V_{IH} = V_{DD}; open drain outputs connected to V_{SS}; all other outputs open. Maximum values: external clock at XTAL1; XTAL2 open. Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
f_{xtal}	clock frequency	see Fig.3	1	–	16	MHz
Oscillator (see Fig.13)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance	V_{DD} = 5 V	3.0	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

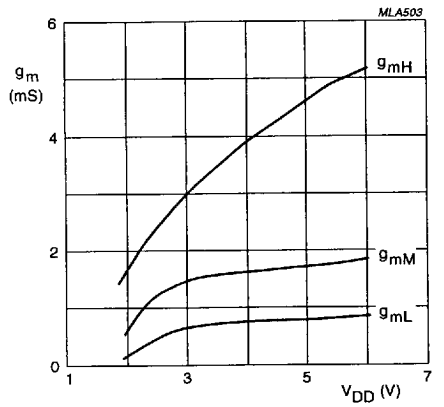


Fig.13 Typical transconductance as a function of supply voltage (V_{DD}) for the options g_{mL}, g_{mM} and g_{mH}.

11.1 I²C-bus interface characteristics

Table 4 I²C-bus timing.

SYMBOL	PARAMETER	INPUT (see Fig.14)	OUTPUT (see Fig.15; note 1)
SCLK			
$t_{HD;STA}$	START condition hold time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF+9}{2 \times f_{xtal}}$
t_{LOW}	SCLK LOW time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF-3}{2 \times f_{xtal}}$; note 2
t_{HIGH}	SCLK HIGH time	$\geq \frac{17}{f_{xtal}}$	$\frac{DF+3}{2 \times f_{xtal}}$; note 2
t_{RC}	SCLK rise time	≤ 1 µs	≤ 1 µs; note 3
t_{FC}	SCLK fall time	≤ 0.3 µs	≤ 0.1 µs; note 4
SDA			
t_{BUF}	bus free time	$\geq \frac{14}{f_{xtal}}$	≥ 4.7 µs; note 5
$t_{SU,DAT}$	data set-up time	≥ 250 ns	$\geq \frac{15}{f_{xtal}}$; note 6
$t_{HD;DAT}$	data hold time	≥ 0	$\geq \frac{9}{f_{xtal}}$
t_{RD}	SDA/P2.3 rise time	≤ 1 µs	≤ 1 µs; note 3
t_{FD}	SDA/P2.3 fall time	≤ 0.3 µs	≤ 0.1 µs; note 4
$t_{SU,STO}$	STOP condition set-up time	$\geq \frac{14}{f_{xtal}}$	$\frac{DF-3}{2 \times f_{xtal}}$

Notes

1. DF stands for divisor of f_{xtal} (see *"PCD33XXA family data sheet"*).
2. Values given for ASC = 0; for ASC =1: $t_{HIGH} = \frac{3(DF+1)}{4 \times f_{xtal}}$; $t_{LOW} = \frac{DF-3}{4 \times f_{xtal}}$.
3. Determined by I²C-bus capacitance (C_b) and external pull-up resistor.
4. At maximum allowed I²C-bus capacitance $C_b = 400$ pF.
5. Determined by program.
6. If $t_{LOW} < \frac{24}{f_{xtal}}$, $t_{SU:DAT} \geq \frac{t_{LOW} - 9}{f_{xtal}}$, independent of ASC.

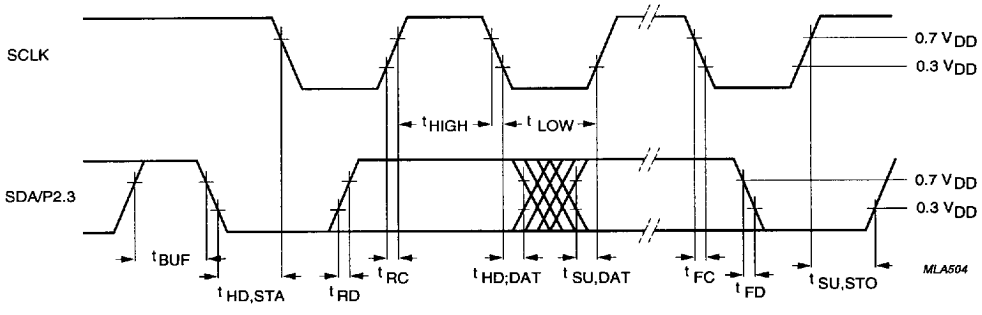


Fig.14 Slave SCLK and receiver SDA/P2.3 timing (SCLK and SDA/P2.3 are inputs).

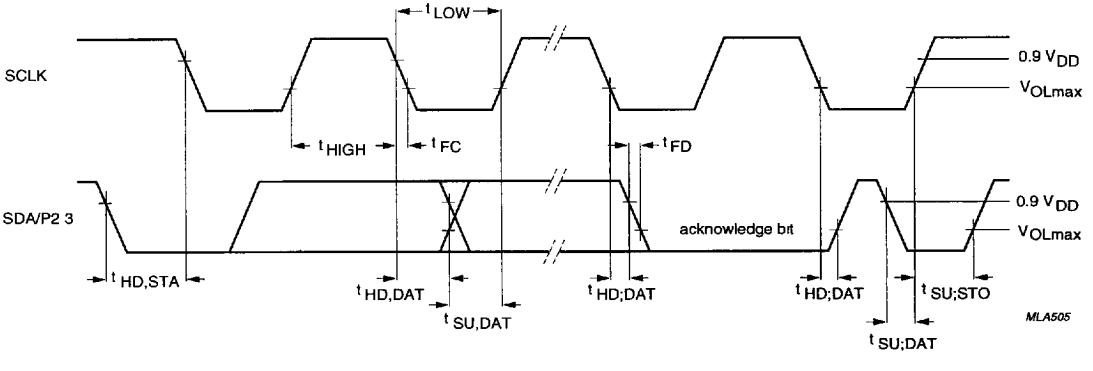
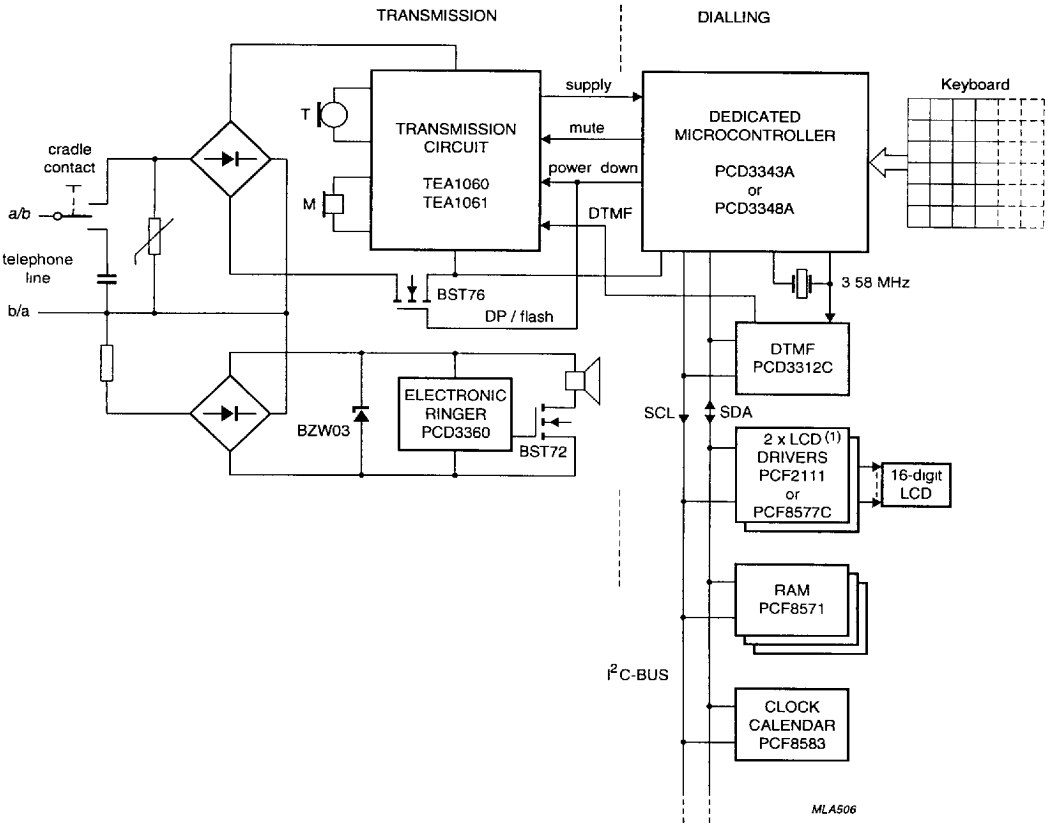


Fig.15 Master SCLK and transmitter SDA/P2.3 timing (SCLK and SDA/P2.3 are outputs).

12 APPLICATION INFORMATION

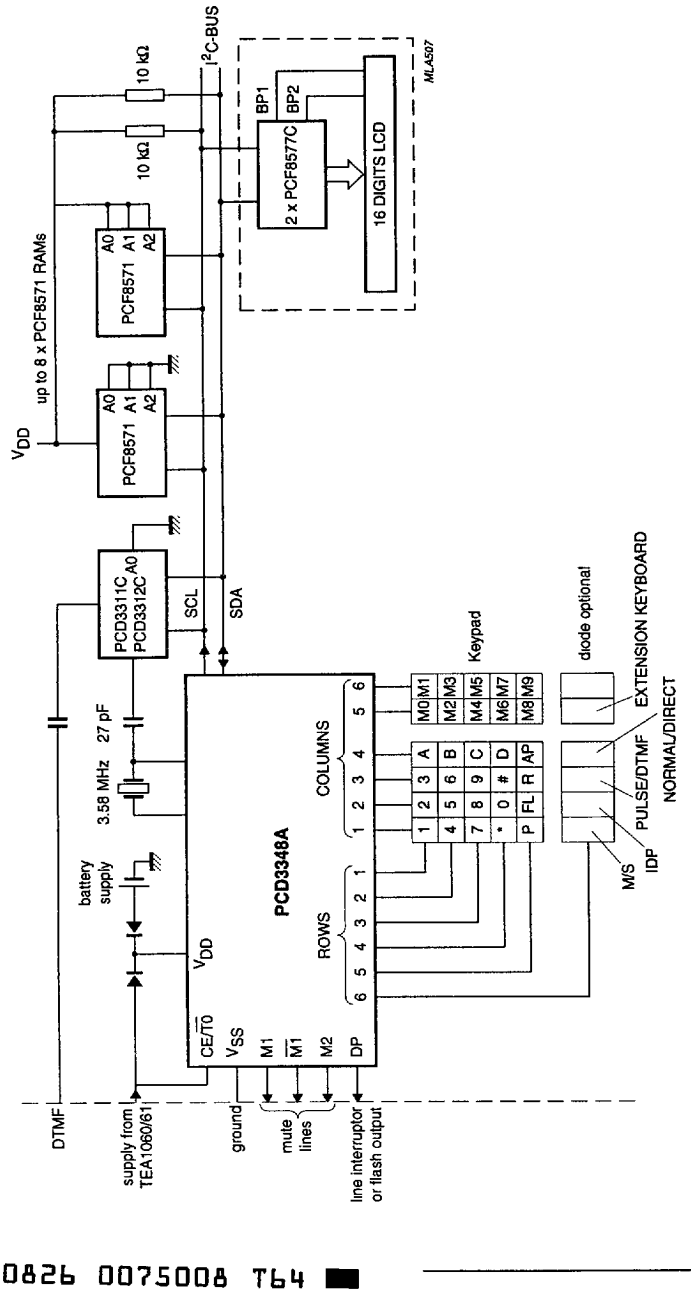
A block diagram of an electronic feature-phone built around the PCD3343A/48A is shown in Fig.16. It comprises the following dedicated telecom ICs:

- TEA1060/1061: transmission circuit for telephony
- PCD3312C: DTMF generator with I²C-bus interface
- PCF2111 or PCF8577C: 2 LCD drivers in LCD module MB7020160
- PCF8571: 1 kbyte RAMs with I²C-bus interfaces
- PCD3360/3361: programmable multi-tone ringer.



(1) Maximum 8.

Fig.16 Block diagram of an electronic feature-phone with common line interface.



A more detailed schematic of the PCD3343A/48A with: PCD3312 (DTMF), two PCF8571 (RAMs) and two PCF2111 (LCD drivers).
Row 5 of the keyboard contains the following special keys:
P: program and autodial
FL: flash or register recall
R: redial or extended redial
AP: access pause
Row 6 contains the different diode options. Columns 5 and 6 contain the keys M0 to M9 used as single name keys for repertory telephone numbers.

Fig.17 PCD3343A/PCD3348A application for an electronic feature-phone with associated keyboard.