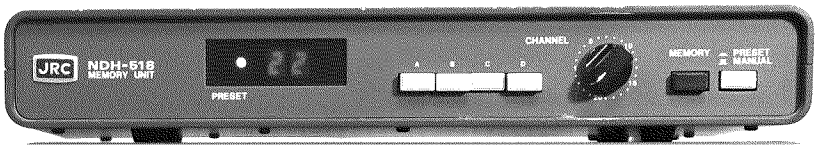
SERVICE MANUAL
FOR
MODEL NDH-518 MEMORY UNIT



JRC

Japan Radio Co., Ltd.

SERVICE INSTRUCTIONS : NDH518 MEMORY UNIT

GENERAL

The block diagram and schematic for the memory unit are shown in the appendix. The unit is made up of a memory circuit utilising six integrated circuits type μPD5101LC. These IC's are 1K CMOS static RAM (256 x 4) where the FF is used to store data, clocks are not needed, and the information stays in storage as long as power is supplied. It should be noted that an optional battery(s) can be installed to back up data stored.

Important - Alkaline batteries should be used as commonly used manganese types will possibly leak when they become exhausted. Any consequent damage is not covered by warranty.

Frequency data is transferred from the receiver via the three state buffers (IC 9, 10, 11, 12, 13, 14).

Data input and memory output is via the cable terminated with the plug P4.

96 frequencies can be put in memory (24 channels per channel switch x 4 - A, B, C, D, selected by the push button switches).

The channel is designated by specifying the address of the RAM's by the channel switches and this information is simultaneously sent to the channel display circuit, IC7 and IC3.

The power source voltage detecting circuit controls the chip enable terminal of the RAM's in order to protect the memory frequency data from being lost when the power switch is turned off.

The power detecting circuit is TR2/IC16.

POWER

Since CMOS is used, power supply requirements are low. 10-11V from the receiver is supplied through P4 and P7/J7 pin 2,3 and regulated to 5V through IC17.

DATA - TESTING

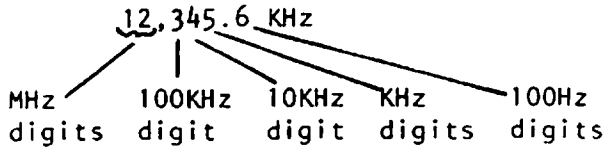
The table below shows the INPUT state of data from the receiver for each of the digits that are capable of being displayed on the receiver. Levels for all digits representing 100Hz, 1KHz, etc. are similar, the exception being the digits representing tens of MHz and the 20MHz digit.

If incorrect levels are being returned from the memory resulting in an incorrect display, isolation of the faulty digit(s) may be made by comparing actual level on the apropriate pins of J7.

PROCEDURE

1. Set the receiver in manual.
2. Check with logic tester to see if the levels are according to the following table as each digit is selected. Increment the tuning

knob or band switch as required to access the digits corresponding to their place in the dialled up frequency, e.g.



J7 PINS

100Hz UNITS	5	6	7	8
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = HIGH ≈ 5V

Similar levels will be evident for KHz, tens KHz, and 100KHz digits.
1KHz Pins are on J7 Pins 9 and 10, J6 Pins 1 and 2
10KHz Pins are on J6 Pins 3,4,5 and 6
100KHz Pins are on J6 Pins 7,8,9 and 10
Levels for 1MHz are on J5 Pins 1,2,3 and 4

Note: Levels will be same as in 100Hz sample chart as above, with pins taken in sequence listed.

For tens of MHz, J5 pin 9 is "High" for a reading of "1", and pin 8 is "High" for a reading of "2".

MEMORY IC

Levels noted on all pins including the supply rail for IC 1,2,3,4,5 and 6 are shown in the table below.

TEST CONDITIONS

1. Dial up a frequency of 12,345.6 MHz on the receiver, with memory unit connected.
2. Select CH1, depress button "A" and "preset" button.
3. Check levels per table below.

PINS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
IC1	L	L	L	H	L	H	H	L	H	H	L	L	H	H	H	H	H	L	L	H	L	H
IC2	L	L	L	H	L	H	H	L	L	L	H	H	L	L	L	L	H	L	L	H	L	H
IC3	L	L	L	H	L	H	H	L	0	H	H	H	L	L	L	L	H	L	L	H	L	H
IC4	L	L	L	H	L	H	H	L	L	L	L	L	H	H	L	L	H	L	L	H	L	H
IC5	L	L	L	H	L	H	H	L	H	H	L	L	H	H	L	L	H	L	L	H	L	H
IC6	L	L	L	H	L	H	H	L	L	L	H	H	H	H	L	L	H	L	L	H	L	H

Levels for the three state buffer IC's, IC 9,10,11,12,13 and 14 are shown on the table below. Frequency reading on the receiver is 12,345.6 MHz.

	PINS													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
IC9	H	H	H	H	L	L	L	H	H	H	H	H	H	H
IC10	H	L	L	H	H	H	L	L	L	H	L	L	H	H
IC11	H	H	0	H	H	H	L	L	L	H	L	L	H	H
IC12	H	L	L	H	L	L	L	H	H	H	L	L	H	H
IC13	H	H	H	H	H	L	L	H	H	H	L	L	H	H
IC14	H	L	L	H	H	H	L	H	H	H	L	L	H	H

COMPONENTS

1. Parts list for the NDH518 is appended.
2. Schematic diagram.
3. Block diagram.
   IC's specifications of the major IC used in the memory unit are also appended.

Testing

How do you know whether the I/O works OK, and all is well with the data bits?
Are all address lines all well connected?

Fill channel 1 to 10 of bank A with:

Chan	figures	binary
1	11.111.1	0001
2	22.222.2	0010
3	3.333.3	0011
4	4.444.4	0100
5	5.555.5	0101
6	6.666.6	0110
7	7.777.7	0111
8	8.888.8	1000
9	9.999.9	1001
10	10.000.0	0000

First test

Choose Bank A (all switches adresbit B, C and D would be dis-engaged, contact problems with those adresbit pull-down than not applicable)
With the table left you quickly see whether there are any address or data bit errors.

Because never programmed channels can contain invalid data noise, you can see the strangest characters or dark spots on the display prior to a real channel MEM write action. This is normal and NOT worrying!
So do: → tune in something → press MEM → press Preset → identical? → OK.

You can quickly erase all noise everywhere: set tune to 000.0, hold MEM, and rotate 24 steps quickly, everything is reset to 0. Next bank.

After a long standstill, the switches B, C and D may have contact cracking, use intensly or perhaps a tiny drop contact cleaner or spray?

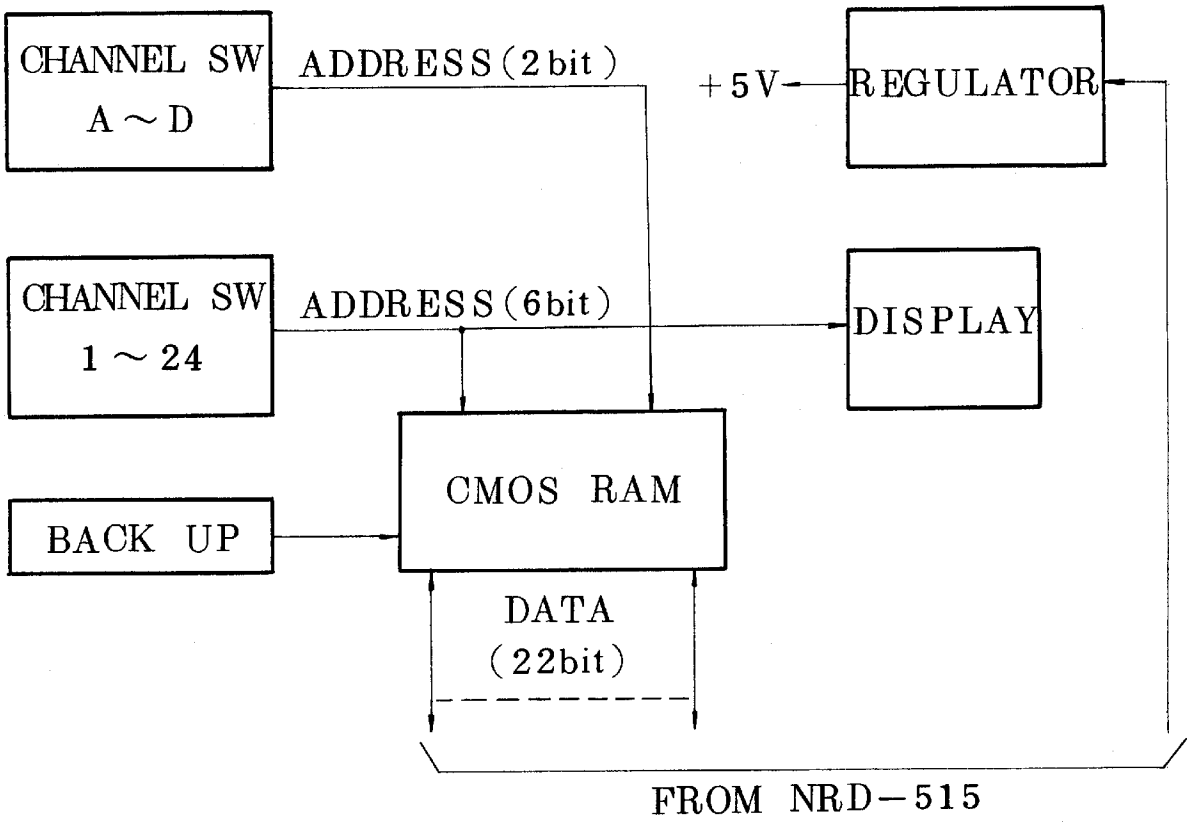


Fig. 1 Block diagram of NDH-518 Memory Unit

図 1　NDH－518 メモリユニット系統図

1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION

The μPD5101L and μPD5101L-1 are very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memories. They meet the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

All inputs and outputs of the μPD5101L and μPD5101L-1 are TTL compatible. Two chip enables ($\overline{CE}_1$, CE_2) are provided, with the devices being selected when $\overline{CE}_1$ is low and CE_2 is high. The devices can be placed in standby mode, drawing 10 μA maximum, by driving $\overline{CE}_1$ high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

The μPD5101L and μPD5101L-1 have separate input and output lines. They can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is nondestructively read out. Read mode is selected by placing a high on the R/W pin. Either device is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

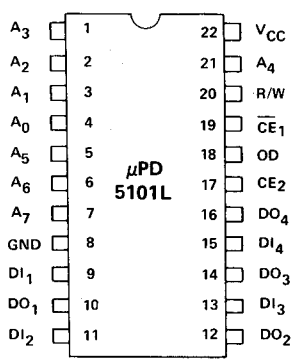
The μPD5101L and μPD5101L-1 are fabricated using NEC's silicon gate complementary MOS (CMOS) process.

3

FEATURES

- Directly TTL Compatible – All Inputs and Outputs
- Three-State Output
- Access Time – 650 ns (μPD5101L); 450 ns (μPD5101L-1)
- Single +5V Power Supply
- CE_2 Controls Unconditional Standby Mode
- For operation at +3V Power Supply, Contact the NEC Sales Office.

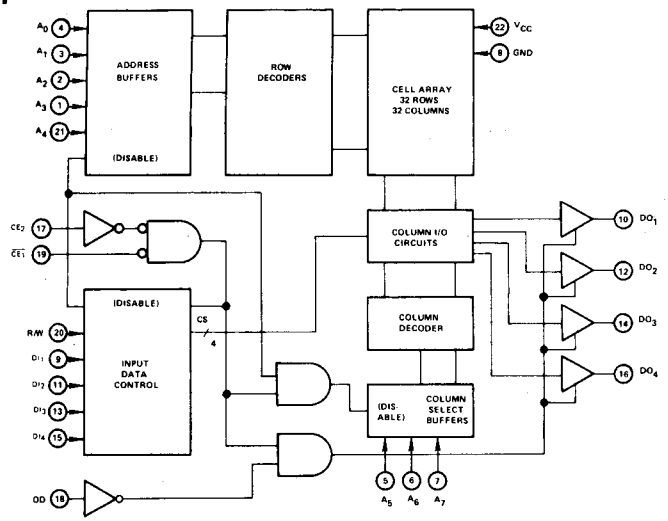
PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_4$	Data Input
$A_0 - A_7$	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$, CE_2	Chip Enables
OD	Output Disable
$DO_1 - DO_4$	Data Output
V_{CC}	Power (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -40°C to +125°C
Voltage On Any Pin With Respect to Ground . . . . . -0.3 Volts to V_{CC} +0.3 Volts
Power Supply Voltage . . . . . -0.3 to +7.0 Volts
T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Leakage	I_{LIH} (2)			1	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL} (2)			-1	μA	V_{IN} = 0V
Output High Leakage	I_{LOH} (2)			1	μA	$\overline{CE}_1$ = 2.2V, $V_{OUT} = V_{CC}$
Output Low Leakage	I_{LOL} (2)			-1	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.0V
Operating Current	I_{CC1}			22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Operating Current	I_{CC2}			27	mA	V_{IN} = 2.2V Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Standby Current	I_{CCL} (2)			10	μA	V_{IN} = 0 to 5.25V $CE_2 \leq$ 0.2V
Input Low Voltage	V_{IL}	-0.3		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.0 mA
Output High Voltage	V_{OH2}	3.5			V	I_{OH} = -100 μA

Notes: (1) Typical values at T_a = 25°C and nominal supply voltage.
(2) Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance (All Input Pins)	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0V

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Read Cycle	t_{RC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Access Time	t_A			650			450	ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}			600			400	ns	Timing measurement reference level: 1.5 Volt
Chip Enable (CE_2) to Output	t_{CO2}			700			500	ns	Output load: I_{TTL}
Output Disable to Output	t_{OD}			350			250	ns	Gate and C_L = 100 pF
Data Output to High Z State	t_{DF}	0		150	0		130	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0			0			ns	
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0			0			ns	

3

WRITE CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Write Cycle	t_{WC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Write Delay	t_{AW}	150			130			ns	
Chip Enable ($\overline{CE_1}$) to Write	t_{CW1}	550			350			ns	Input rise and fall times: 20 ns
Chip Enable (CE_2) to Write	t_{CW2}	550			350			ns	Timing measurement reference level: 1.5 Volt
Data Setup	t_{DW}	400			250			ns	Output load: I_{TTL}
Data Hold	t_{DH}	100			50			ns	Gate and C_L = 100 pF
Write Pulse	t_{WP}	400			250			ns	
Write Recovery	t_{WR}	50			50			ns	
Output Disable Setup	t_{DS}	150			130				

LOW V_{CC} DATA RETENTION CHARACTERISTICS

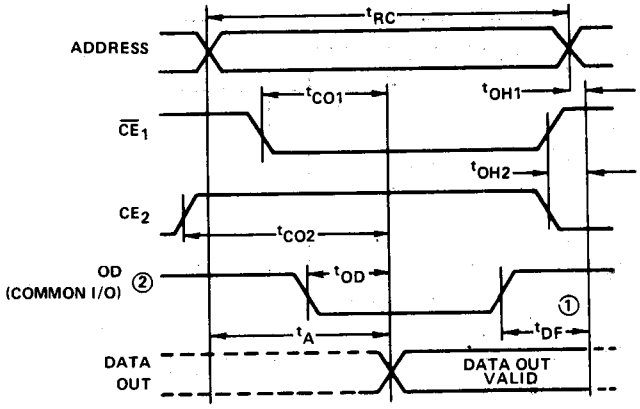
T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leq +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	V_{CCDR} = +2.0V $CE_2 \leq +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC}①			ns	

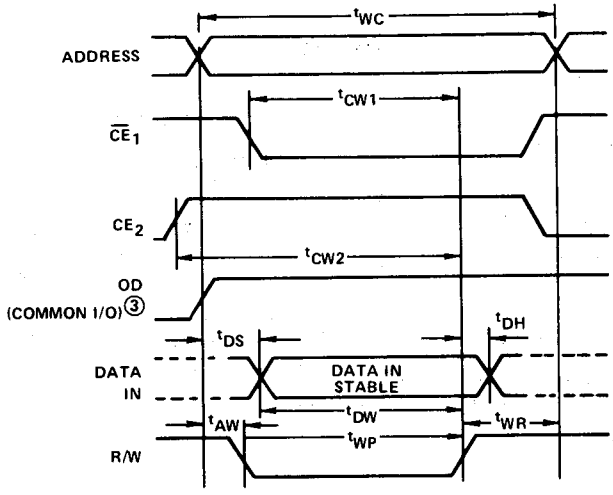
Note: ① t_{RC} = Read Cycle Time

TIMING WAVEFORMS

READ CYCLE

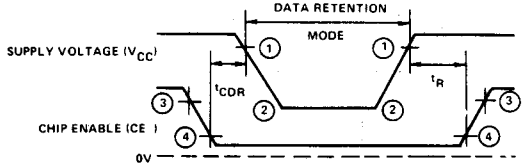


WRITE CYCLE



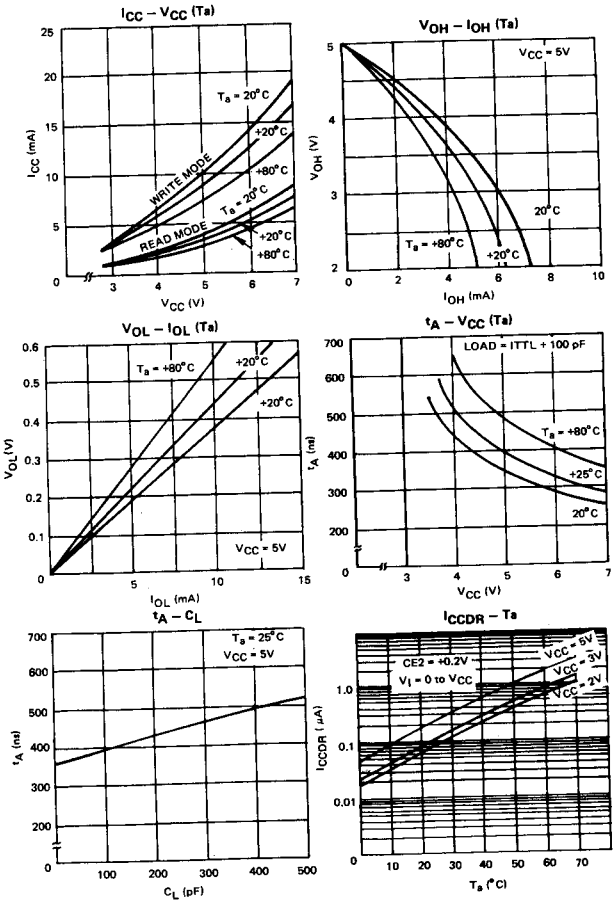
Notes: ① Typical values are for T_a = 25°C and nominal supply voltage.
② OD may be tied low for separate I/O operation.
③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

LOW V_{CC} DATA RETENTION

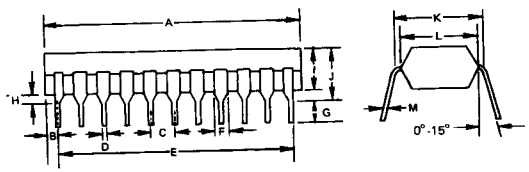


Notes: ① 4.75V
② V_{CCDR}
③ V_{IH}
④ 0.2V

TYPICAL OPERATING CHARACTERISTICS



PACKAGE OUTLINE μPD5101LC



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 0.10	0.02 0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	0.25 +0.10 0.05	0.01 +0.004 0.002

5101LDS-REV1-12-81-CAT

256 × 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5101 is a very low-power 1024-bit static CMOS random access memory, organized as 256 words by 4 bits. It is suitable for low power and high speed applications where battery standby power is required to ensure non-volatility of data. All inputs and outputs are fully TTL compatible and pinning is compatible with 2101-type NMOS static RAMs and 5101-type CMOS static RAMs.

There are two chip enable inputs, $\overline{CE1}$ and CE2, selection being made when $\overline{CE1}$ is LOW and CE2 is HIGH. The memory has an output disable function, OD, which allows the inputs/outputs to be used separately, or to be tied together for use in common data I/O systems.

Features

- Operating supply voltage range — 2,5 to 5,5 V
- Low data retention voltage — min. 1 V
- Low power consumption in both operating and standby modes
- Access time 150 ns at V_{DD} = 5 V; 400 ns at V_{DD} = 3 V
- Three-state outputs
- All inputs and outputs directly TTL compatible
- Choice of two package types

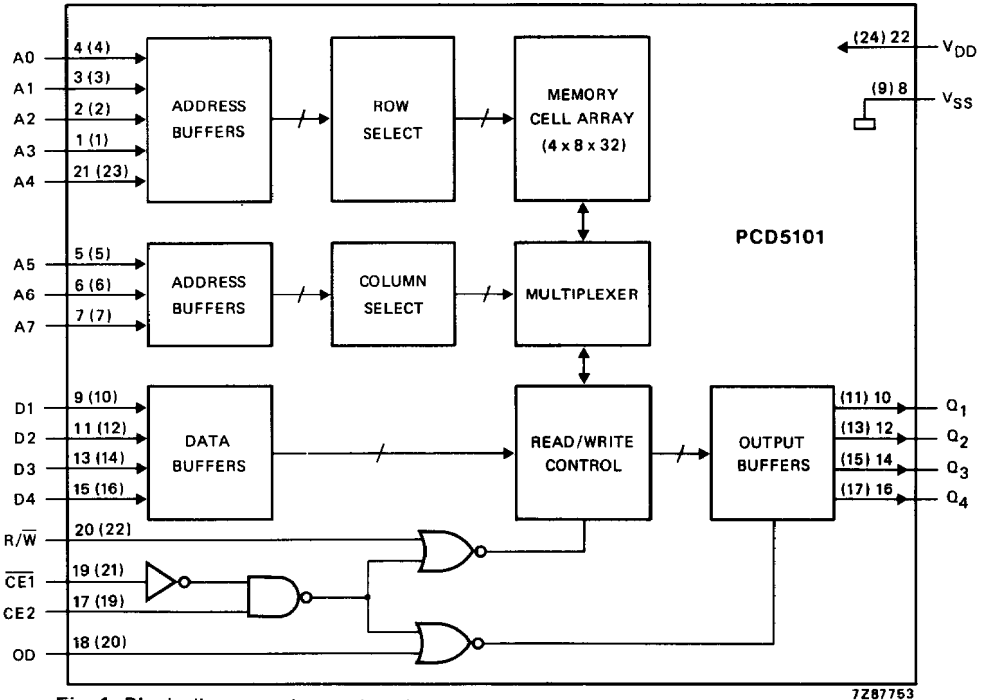


Fig. 1 Block diagram: pin numbers in parentheses are for PCD5101T; other pin numbers are applicable to PCD5101P.

PACKAGE OUTLINES

PCD5101P: 22-lead DIL; plastic (SOT116).
PCD5101T: 24-lead mini-pack; plastic (SO24; SOT137A).

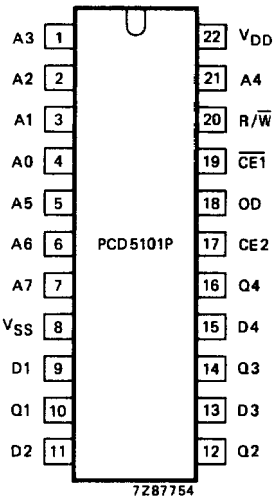


Fig. 2 Pinning diagram for PCD5101P.

PINNING

D1, D2, D3, D4	data inputs
A0, A1, A2, A3, A4, A5, A6, A7	address inputs
R/$\overline{W}$	read/write input
$\overline{CE1}$, CE2	chip enable inputs
OD	output disable
Q1, Q2, Q3, Q4	data outputs
V_{DD}	positive supply
V_{SS}	negative supply
n.c.	not connected

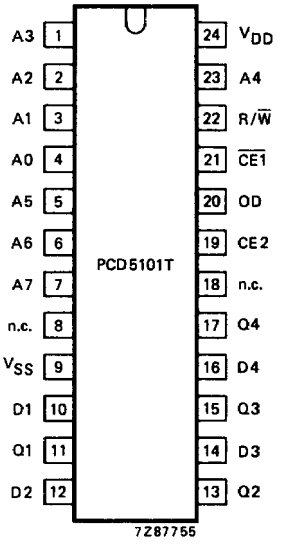


Fig. 3 Pinning diagram for PCD5101T.

OPERATING MODES

Table 1 Mode selection

$\overline{CE1}$	CE2	R/$\overline{W}$	OD	mode of operation	output state
H	X	X	X	standby	high impedance
X	L	X	X	standby	high impedance
L	H	L	H	write	high impedance
L	H	L	L	write	equal to input data
L	H	H	L	read	data valid
L	H	H	H	read	high impedance

Separate input/output: write cycle OD = X; read cycle OD = L.

Common input/output: write cycle OD = H; read cycle OD = L.

H = HIGH voltage level
L = LOW voltage level
X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to 8,0	V
Input voltage range (any pin)	V_I	V_{SS} − 0,3 to V_{DD} +0,3	V
Operating temperature range	T_{amb}	−25 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5,0	5,5	V
Operating supply current					
at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 4,0 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 2,0 mA	V_{OH}	2,4	–	–	V

D.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	3,0	3,5	V
Operating supply current					
at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 or 1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input voltage HIGH	V_{IH}	1,6	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,3	V
Output voltage HIGH at $-I_{OH}$ = 1,0 mA	V_{OH}	1,7	–	–	V

A.C. TEST CONDITIONS (V_{DD} = 5 V)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load (2 TTL inputs and load capacitance C_L)	Fig. 4

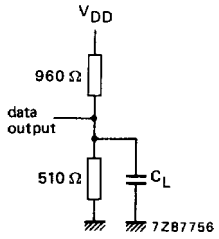


Fig. 4 Test load.

A.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; loads as per Fig. 4 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	150	–	–	ns
Address access time	t_{AA}	–	–	150	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	150	ns
Chip enable CE2 to output	t_{CO2}	–	–	150	ns
Output disable OD to output	t_{OD}	–	–	70	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	70	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	150	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	120	–	–	ns
Chip enable CE2 to write	t_{CW2}	120	–	–	ns
Data set-up time	t_{DW}	70	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	70	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	70	–	–	ns

A.C. TEST CONDITIONS (V_{DD} = 3 V)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	Fig. 5

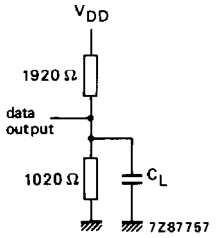


Fig. 5 Test load.

A.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; loads as per Fig. 5 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	400	–	–	ns
Address access time	t_{AA}	–	–	400	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	400	ns
Chip enable CE2 to output	t_{CO2}	–	–	400	ns
Output disable OD to output	t_{OD}	–	–	200	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	200	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	400	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	300	–	–	ns
Chip enable CE2 to write	t_{CW2}	300	–	–	ns
Data set-up time	t_{DW}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	200	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	200	–	–	ns

WAVEFORMS

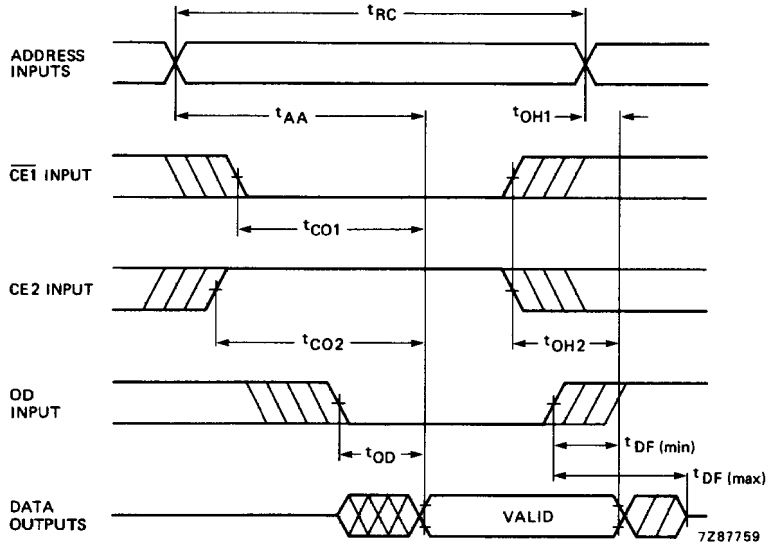


Fig. 6 Read cycle timing; R/$\overline{W}$ = HIGH.

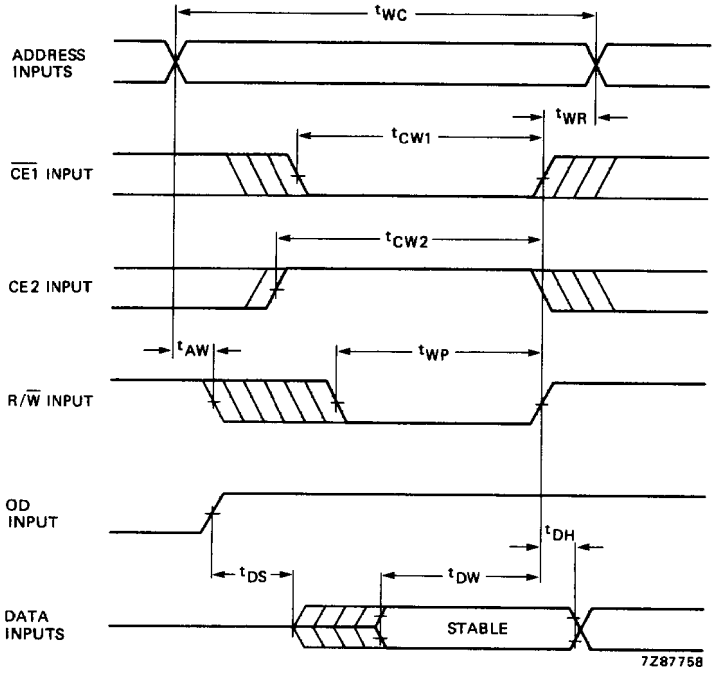


Fig. 7 Write cycle timing.

LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

$CE2 \leqslant 0{,}2$ V; $T_{amb} = -25$ to $+70$ °C.

parameter	symbol	min.	typ.	max.	unit
Supply voltage for data retention	V_{DR}	1,0	–	5,5	V
Data retention current at V_{DD} = 1,5 V	I_{DR}	–	0,02	2,0	μA
Chip deselect to data retention time	t_{CDR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

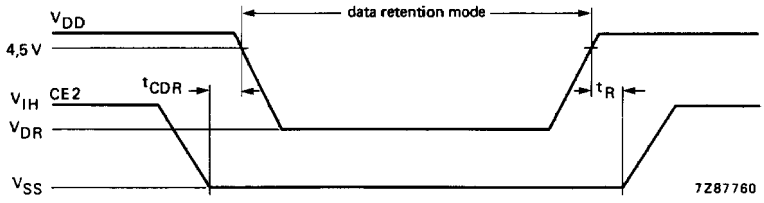


Fig. 8 Low supply voltage data retention characteristics.

PARTS LIST
FOR
MEMORY UNIT
MODEL NDH-518

MARCH, 1982

JRC

Japan Radio Co., Ltd.

PARTS LIST

MEMORY UNIT

MODEL NDH-518

1. MEMORY CDD-206

2. DISPLAY CDE-162

The table lists parts in alphanumeric order of their reference designations "NO." (see abbreviations below),and provides the following information on each part:

A. JRC code number.
B. Type.
C. Description of part.

Ordering information

To obtain replacement parts, address order or inquiry to our Japan Radio CO, LTD. Sales Offices. Identify parts by their JRC code number. To obtain a part that is not listed, included:

A. Equipment model number.
B. Equipment serial number.
C. Description of the part.
D. Function and location of the part.

ABBREVIATIONS

A	Assembly	MIC	Microphone
ANT	Antenna	MG	Motor generator
AR	Arester	MP	Heat dissipating device (heatsink,etc.), mechanical part
AT	Attenuator	MR	Shunt, multiplier
B	Rotary machine	MT	Centering magnet
BEL	Bell	P	Plug
BT	Battery	PC	Printed circuit
BZ	Buzzer	I	Lamp
C	Fixed capacitor	IS	Lamp socket
CB	Circuit breaker	PU	Pick-up
CD	Rectifier,detector,diode,varistor	R	Fixed resistor, thermistor
CV	Variable capacitor	RS	Lead selector
D	Dynamotor	RV	Variable resistor
DC	Directional coupler	S	Switch, key, thermostat, interlock
DL	Delay line	SP	Speaker
E	Earth, ground	T	Transformer
F	Fuse	TB	Terminal board
FL	Filter	TC	Thermocoupler
FS	Fuse holder	TF	Tuning fork
G	Generator, vibrator	TP	Testpoint
HC	Hybrid circuit	TR	Transistor
HR	Thermostatic oven, heater	TRS	Transistor socket
HS	Handset	V	Electron tube
HT	Telephone receiver	VR	Voltage regulator
HY	Hybrid coil	VS	Electron tube socket
IC	Integrated circuit	W	Wire, cable, wave guide
J	Jack	X	Crystal
K	Relay	XD	Discriminator
KS	Relay socket	XS	Crystal socket
L	Inductor, coil	XU	Crystal oscillator
M	Meter	Z	Tuned cavity, pulse forming network, dummy

PARTS LIST

FOLDER	TITLE	LIST NO.	SHEET NO.
	MEMORY	COD-206	1

PART NO.	PART NAME	TYPE	DESCRIPTION	REMARKS	CODE
BTS1	BT HOLDER				6ZZAB01858
BTS2	BT HOLDER				6ZZAB01858
BTS3	BT HOLDER				6ZZAB01858
C1	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C2	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C3	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C4	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C5	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C6	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C7	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C8	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C9	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C10	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C11	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C12	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C13	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C14	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C15	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C16	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C17	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C18	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C19	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C20	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C21	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C22	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C23	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C24	CAP,FXD PLSTC	ECQ-M1H104KZ	0.1UF		5CBAA00123
C25	CAP,FXD EL CTLT	ECE-A1ES100	25V10UF		5CEAA01348
C26	CAP,FXD CER	DD109E103P50V02	50V 10000PF		5CBAB00301
C27	CAP,FXD CER	DD109E103P50V02	50V 10000PF		5CBAB00301
C28	CAP,FXD EL CTLT	ECE-A1ES100	25V10UF		5CEAA01348
C29	CAP,FXD CER	DD109E103P50V02	50V 10000PF		5CBAB00301
C30	CAP,FXD CER	DD109E103P50V02	50V 10000PF		5CBAB00301
C31	CAP,FXD EL CTLT	ECE-A1ES100	25V10UF		5CEAA01348
C32	CAP,FXD CER	DD109E103P50V02	50V 10000PF		5CBAB00301

PARTS LIST

ORDER	TITLE	LIST NO.	SHEET NO.
	MEMORY	CDD-206	2

PART NO.	PART NAME	TYPE	DESCRIPTION	REMARKS	CODE
C33	CAP,FXD EL CTLT	ECE-A1ES100	25V10UF		5CEAA0134P
C34	CAP,FXD EL CTLT	ECE-A1ES101	25V100UF		5CEAA0134C
C35	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C36	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
C37	CAP,FXD CER	DD112SL102J50V02	50V 1000PF		5CAAA01112
CD4	DIODE	1DD2	200V 1A		5TXAG00001
CD5	DIODE	1S1588LB-10			5TXAD00248
CD6	DIODE	1S1588LB-10			5TXAD00249
CD7	DIODE	HZ3HC1			5TXAE00119
CD8	DIODE	1DD8			5TXAG00002
IC1	IC	UPD5101LC			5DDAC00151
IC2	IC	UPD5101LC			5DDAC00151
IC3	IC	UPD5101LC			5DDAC00151
IC4	IC	UPD5101LC			5DDAC00151
IC5	IC	UPD5101LC			5DDAC00151
IC6	IC	UPD5101LC			5DDAC00151
IC7	IC	HD74LS47P			5DDAF00390
IC8	IC	HD74LS47P			5DDAF00390
IC9	IC	SN74LS126AN			5DDAL00422
IC10	IC	SN74LS126AN			5DDAL00422
IC11	IC	SN74LS126AN			5DDAL00422
IC12	IC	SN74LS126AN			5DDAL00422
IC13	IC	SN74LS126AN			5DDAL00422
IC14	IC	SN74LS126AN			5DDAL00422
IC15	IC	TC4049BP			5DDAS00044
IC16	IC	TC4049BP			5DDAS00044
IC17	IC	HA17805P			5DAAG00067
J1	CONNECTOR	PCN6-20PA-2.5DS	20P		5JDAA00049
J5	CONNECTOR	HNC2-2.5P-10DS	10P		5JDAA00275
J6	CONNECTOR	HNC2-2.5P-10DS	10P		5JDAA00275
J7	CONNECTOR	HNC2-2.5P-10DS	10P		5JDAA00275
K1	RELAY	NF-HD-5V			5KLAD00038
L1	COIL	LF1-100K	10UH		5LCAB00001
P4	CONNECTOR	H-67CJD00012			6ZCJD00012
P5	CONNECTOR	HNC2-2.5S-10	10P		5JDAA00277

PARTS LIST

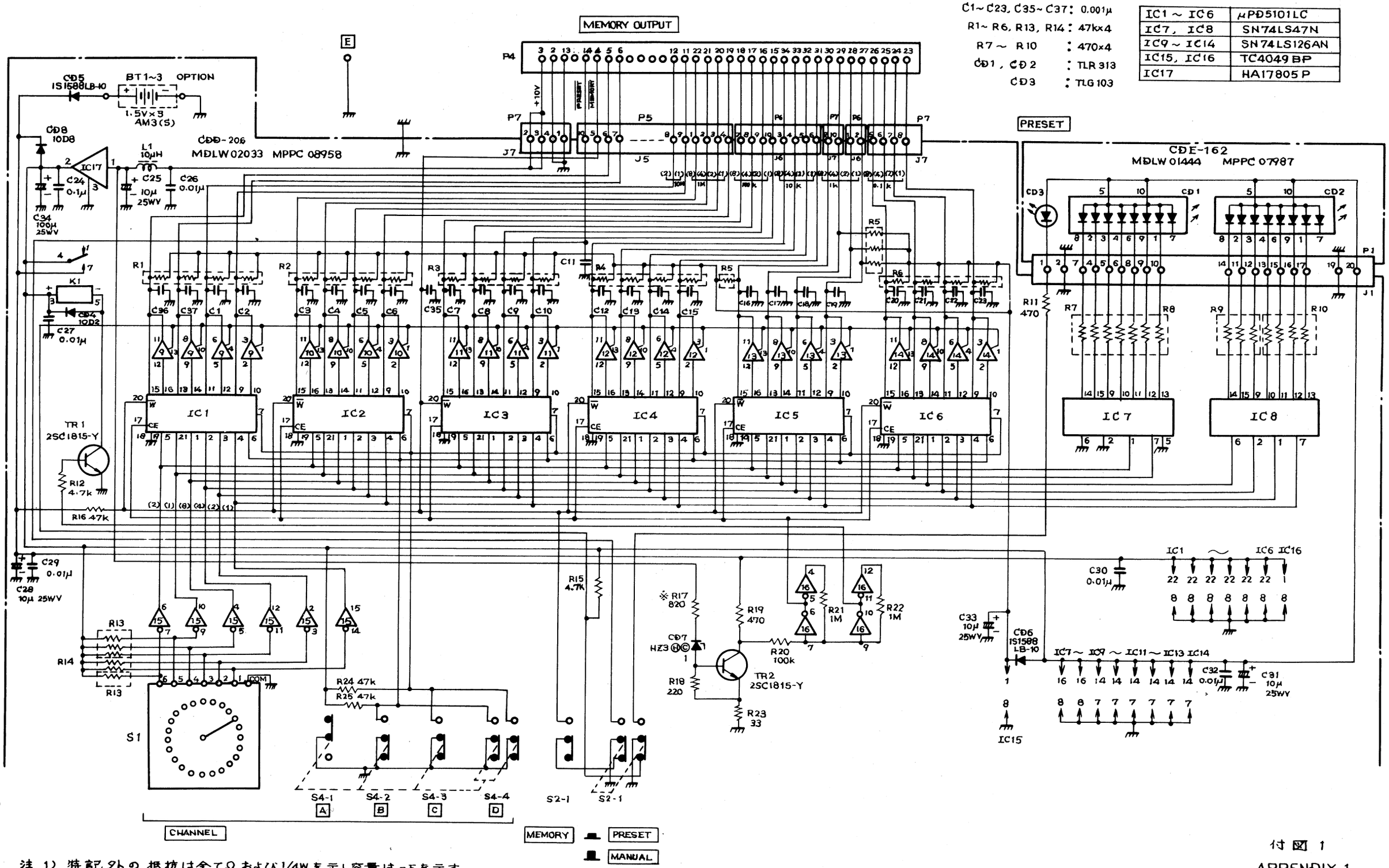
CODE	TITLE	LIST NO.	SHEET NO.
	MEMORY	CDD-206	3

PART NO.	PART NAME	TYPE	DESCRIPTION	REMARKS	CODE
P6	CONNECTOR	HNC2-2.5S-10	10P		5JDAA00277
P7	CONNECTOR	HNC2-2.5S-10	10P		5JDAA00277
PC1	PCB	MPPC08958			MPPC08958
R1	RESISTOR	IHR-1/8-4-473JA	1/8W 47K OHM X4		5RZAB0002C
R2	RESISTOR	IHR-1/8-4-473JA	1/8W 47K OHM X4		5RZAB0002C
R3	RESISTOR	IHR-1/8-4-473JA	1/8W 47K OHM X4		5RZAB0002C
R4	RESISTOR	IHR-1/8-4-473JA	1/8W 47K OHM X4		5RZAB0002C
R5	RESISTOR	IHR-1/8-4-473JA	1/8W 47K OHM X4		5RZAB0002C
R6	RESISTOR	IHR-1/8-4-473JA	1/8W 47K OHM X4		5RZAB0002C
R7	RESISTOR	IHR-1/8-4-471JA	1/8W 470 OHM X4		5RZAB00024
R8	RESISTOR	IHR-1/8-4-471JB	1/8W 470 OHM X4		5RZAB00024
R9	RESISTOR	IHR-1/8-4-471JB	1/8W 470 OHM X4		5RZAB00024
R10	RESISTOR	IHR-1/8-4-471JB	1/8W 470 OHM X4		5RZAB00024
R11	RESISTOR FXD	ERD-25UJ471	1/4W 470 OHM		5RDAA01337
R12	RESISTOR FXD	ERD-25UJ472	1/4W 4.7K OHM		5RDAA01361
R13	RESISTOR	IHR-1/8-4-473JA	1/8W 47K OHM X4		5RZAB0002C
R14	RESISTOR	IHR-1/8-4-473JA	1/8W 47K OHM X4		5RZAB0002C
R15	RESISTOR FXD	ERD-25UJ472	1/4W 4.7K OHM		5RDAA01361
R16	RESISTOR FXD	ERD-25UJ473	1/4W 47K OHM		5RDAA01385
R17	RESISTOR FXD	ERD-25UJ102	1/4W 1K OHM		5RDAA01345
R18	RESISTOR FXD	ERD-25UJ221	1/4W 220 OHM		5RDAA01329
R19	RESISTOR FXD	ERD-25UJ471	1/4W 470 OHM		5RDAA01337
R20	RESISTOR FXD	ERD-25UJ104	1/4W 100K OHM		5RDAA01393
R21	RESISTOR FXD	ERD-25UJ105	1/4W 1M OHM		5RDAA01417
R22	RESISTOR FXD	ERD-25UJ105	1/4W 1M OHM		5RDAA01417
R23	RESISTOR FXD	ERD-25UJ330	1/4W 33 OHM		5RDAA01305
R24	RESISTOR FXD	ERD-25UJ473	1/4W 47K OHM		5RDAA01385
R25	RESISTOR FXD	ERD-25UJ473	1/4W 47K OHM		5RDAA01385
S1	SWITCH	H-6SSJD00014	6BITS L=30MM		6SSJD00014
S2	SWITCH	H-6SCJD00115			6SCJD00115
S4	SWITCH	H-6SCJD00114			6SCJD00114
TR1	TRANSISTOR	2SC1815-Y			5TCAF00219
TR2	TRANSISTOR	2SC1815-Y			5TCAF00219

PARTS LIST

CODE?	TITLE	LIST NO.	SHEET NO.
	DISPLAY	CDE-162	1

PART NO.	PART NAME	TYPE	DESCRIP-TION	REMARKS	CODE
CD1	LED	TLR313			5TZA000003
CD2	LED	TLR313			5TZA000003
CD3	LED	TLG103	GREEN		5TZA000023
P1	CONNECTOR	PCN6-20S-2.5DS			5JDAA03080
PC2	PCB	MPPC07987			MPPC07987



注 1) 特記外の抵抗は全てΩおよび1/4Wを示し容量はpFを示す。
2). ※印は調整用部品を示す。

NOTES 1. UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICRO-MICRO FRADS.
2. ※ VALUES SELECTED IN MANUFACTURE.

付図 1
APPENDIX 1

NDH-518
メモリユニット接続図
MEMORY UNIT SCHEMATIC DIAGRAM

1/1